

Performance Analysis of DRAM Cell Design on Different Technologies

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Abstract— In this paper power dissipation and area analysis for DRAM cell design has been presented. Many advanced processors now have on chip instructions and data memory using DRAMs. Thus, improving the power efficiency of a DRAM cell is critical to the overall system power dissipation. In this paper DRAM Cell has been designed and simulated using 45 nm and 90 nm technologies. The performance has been compared on both the technologies in terms of area and power consumption. The schematic of DRAM has been developed using DSCH and its layout has been created using Microwind. It can be observed from simulated results that 45 nm based DRAM Cell has consumed less power as compared to 90 nm technology.

Index Terms— DRAM Cell, MOS, RAM, SRAM, VLSI.

I. INTRODUCTION

Semiconductor memories are most important microelectronics component of digital logic system design, such as microprocessors and computers based application ranging from satellites to consumer electronics. Semiconductor memory arrays capable of storing large digital information. The amount of memory required in a particular system depends on the type of application. The ever increasing demand for large storage capacity has driven the fabrication technology and memory development towards more compact design rules and consequently towards higher data storage densities [1]. On-chip memory arrays have become widely used subsystems in VLSI circuits. The semiconductor memory is generally classified according to the type of data storage and data access. Random access memory (RAM) or Read/Write memory permit the modification of data stored in the memory array. The stored data is volatile i.e. it is lost when power supply is turned off.

A computer uses RAM to temporarily hold instructions and data for CPU processing tasks. In networking equipment, memory is used to buffer information. Based on the type of storage cell, RAM is classified into two categories: dynamic RAM (DRAM) & static RAM (SRAM). SRAM cell consists of a Latch to store data as long as power is on and refresh operation is not needed [2]. DRAM cell consists of a capacitor to store binary data and a transistor to access the capacitor.

The rest of the paper is organized as follows. Introduction of DRAM cell is explained in section II. Schematic of DRAM cell using 3 CMOS transistors is presented in section III. Results & Discussions are given in section IV. Concluding remarks are given in section V.

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II. DYNAMIC RANDOM ACCESS MEMORY (DRAM)

DRAM is widely used for the main memory in workstations and computers. In this paper we have taken a DRAM cell in two different technologies. Read and write operation for single bit storage is shown by simulating it on DSCH tool and then compare it on the basis of power consumption and surface area. With the variation of channel width of transistor, power consumption variation is also shown in table 1. DRAMs provide very high-density storage. It is 'dynamic' because the leakage phenomenon in DRAM degrades the charge stored in the memory cell with time and makes the periodic refreshment necessary in order to retain data [3].

As the continuing trend for high density memories requires small memory cell sizes, the dynamic RAM cell with a small structure has become a popular choice, where binary data are stored as a charge in a capacitor and the presence or absence of stored charge determines the value of the stored bit.

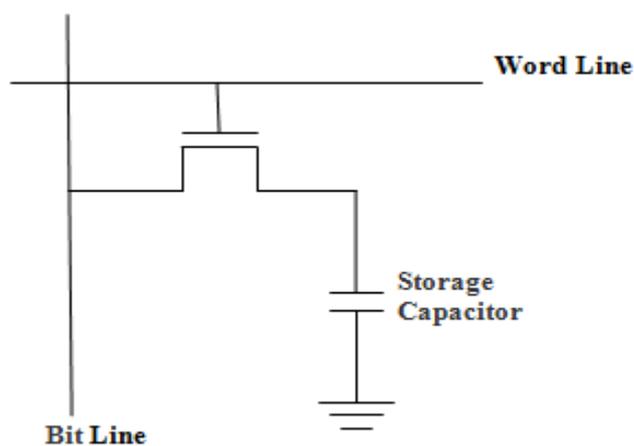


Figure 1. Standard DRAM Cell

The data stored in a capacitor cannot retain indefinitely, because the leakage current modify the stored data. Thus the DRAM cell requires a periodic refreshing of the stored data, so that unwanted modifications due to leakage are prevented before they occur [1]. The usage of a capacitor as a primary storage device generally enables the DRAM cell to be realized in a much smaller silicon area compared to the typical SRAM cell [4]. DRAM (Dynamic Random Access Memory) must be refreshed periodically. It's a Volatile in nature means loses data when power is removed.

The one-transistor DRAM cell has become the industry-standard dynamic RAM cell in high-density DRAM arrays [5]. It has explicit storage capacitor as shown in figure 1. It means that a separate capacitor must be manufactured for

each storage cell, instead of relying on the gate and diffusion capacitances of the transistors for data storage.

III. SCHEMATIC OF DRAM CELL

The three transistor DRAM cell uses a single transistor as the storage device and two transistors each for the Read & Write operation. During Write operation, the write word line is activated and voltage of write bit line is passed on to the gate through transistor. In Read operation, the voltage of read bit line is discharged through other two transistors when gate voltage is high[1].Figure 2 shows the circuit diagram of DRAM cell.It uses three NMOS transistors[6].Layout diagram is shown in Figure 4 and 5.

In 'Write' operation, a word line is enabled and complementary data is written from a pair of bit lines.Charge is stored at the parasitic and gate capacitance of a node connected with a high voltage line. Since no current path is provided to the storage nodes for restoring the charge lost due to leakage, the cell must be refreshed periodically[2].

In 'Read' operation, the voltage of a bit line is discharged to the ground through the transistor where the gate is charged with the high voltage as shown in figure 3. The 'Read' operation is non-destructive since the voltage stored at the node is maintained during the read operation.

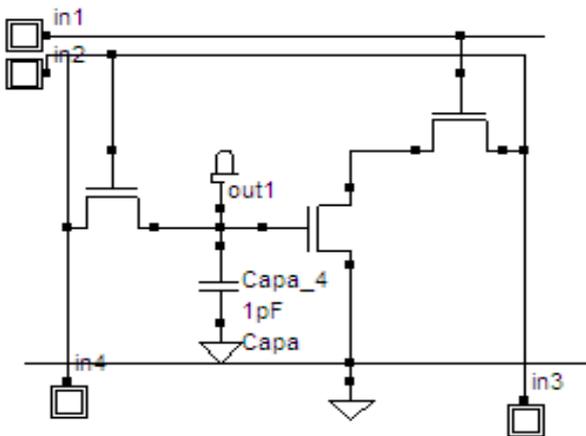


Figure 2. Schematic of DRAM cell

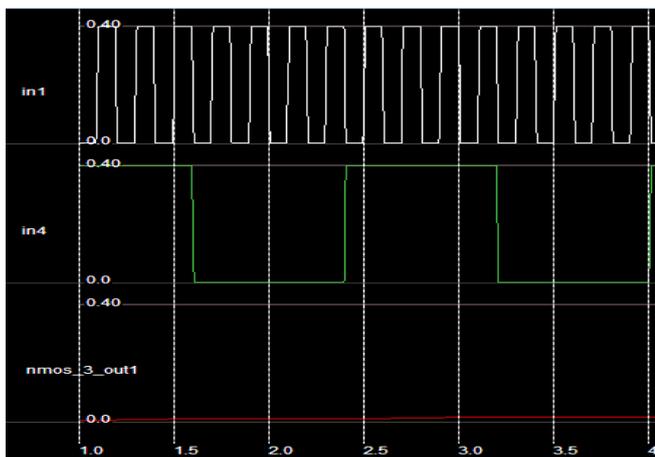


Figure3. Waveforms of DRAM cell

IV. RESULTS & DISCUSSIONS

In this paper we have implemented three transistor DRAM on two different technologies-45 nm and 90 nm and their layouts are presented to compare area in both the technologies.Simulation is done using Microwind 3.1 and DSCH tool[4]. Table 1 shows the area and power dissipation results in 45 and 90 nm technologies.

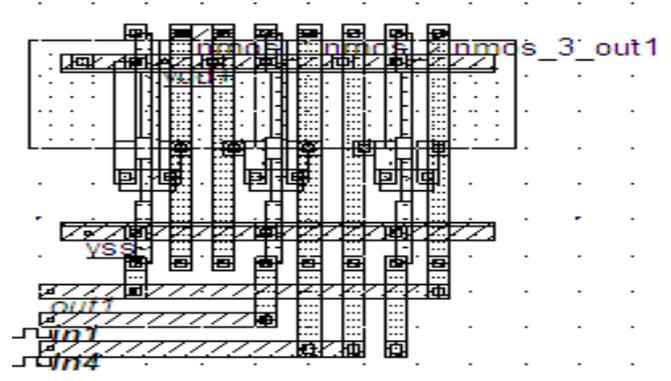


Figure 4. Layout of DRAM Cell in 90 nm technology

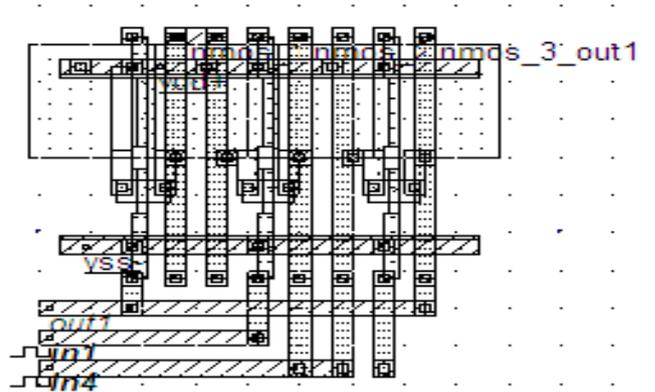


Figure 5. Layout of DRAM Cell in 45 nm technology

Technology	Power Dissipation in DRAM	Area in DRAM
90 nm	6 nW	Width:4.5 μm (90 lambda) Height:4.6 μm (92 lambda) Area:20.7 μm ²
45 nm	1 nW	Width:2.3 μm (90 lambda) Height:2.3 μm (92 lambda) Area:5.2 μm ²

Table 1. Power Dissipation and Area results in DRAM Cell

V. CONCLUSION

We observed that Power dissipation decreases as the technology decreases. It means that as the width of transistor used in particular memory cell increases power consumption also increases. We have taken here optimum width at which the power consumption is minimum. It can be observed from simulated results that 45 nm based DRAM Cell has consumed less power as compared to 90 nm technology. In terms of surface area, 45 nm technology has occupied lesser area as compared to 90 nm technology.

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