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Analyzing the Bit Error Rate & Hardware Implementation of Convolution Encoder & Viterbi Decoder

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***Abstract*— A forward error correction technique known as convolution coding with Viterbi decoding was explored here. This Viterbi project is part of the baseband Error control coding. Here in this paper, the basic Viterbi encoder &decoder in behavior model was built and simulated. The main aim of this paper is to implement the RTL level model of Viterbi decoder. With the testing results of behavior model, with minimizing the data path, register size and butterflies in the design, we try to achieve a low silicon cost design. The RTL Viterbi decoder model includes the Branch Metric block, the Add-Compare-Select block, the trace-back block, the decoding block and next state block. With all done, we further understand about the Viterbi decoding algorithm and the DSP implementation methods. Present wireless standard such as third generation (3G) systems, GSM, 802.11A, 802.16 utilize some configuration of convolution coding. Convolution encoding with viterbi decoding is a powerful method for forward error correction. The viterbi algorithm, which is the most extensively employed decoding algorithm for convolution codes. The aim of this paper is to design convolution encoder and viterbi decoder with a constraint length of 3 and code rate of 2/3. This is realized using Verilog HDL.It is simulated and synthesized using Modelsim Altera 10.1d.**

***Index Terms*— convolution encoder, viterbi decoder, look-up table, MATLAb, viterbi algorithm.**

I. INTRODUCTION

In telecommunication and information theory, forward error correction(FEC) also called channel coding is a system of error control for data transmission, whereby the sender adds systematically generated redundant data to its messages, also known as an error correction code(ECC). The carefully designed redundancy allows the receiver to detect and correct a limited number of error occurring anywhere in the message without the need to ask the sender for additional data. FEC gives the receiver an ability to correct errors without needing a reverse channel to request the retransmission data, but this advantage is at the cost of fixed higher forward channel bandwidth. FEC is therefore applied in situations where retransmissions are relatively costly, or impossible such as when broadcasting to multiple receivers. A Viterbi decoder uses the Viterbi algorithm for decoding a bit stream that has been encoded using forward error correction based on a convolution code. There are other algorithms for decoding a convolutional encoded stream (for example, the FANO algorithm). The viterbi algorithm is the most resource-consuming, but it does the maximum likelihood decoding.

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II. METHODOLOGY

Encoder: Designing with HDLs is analogous to computer programming. A textual description with comments is an easier way to develop and debug circuits. This also provides a concise representation of the design, compared to gate-level schematics. Gate-level schematics are almost incomprehensible for very complex designs. HDLs are most certainly a trend of the future. With rapidly increasing complexities of digital circuits and increasingly sophisticated CAD tools, HDLs will probably be the only method for large digital designs. No digital circuit designer can afford to ignore HDL-based design. An encoder is a digital circuit device, transducer, software program, algorithm or person that converts information from one format or code to another, for the purpose of standardization, speed, secrecy, security or compressions.

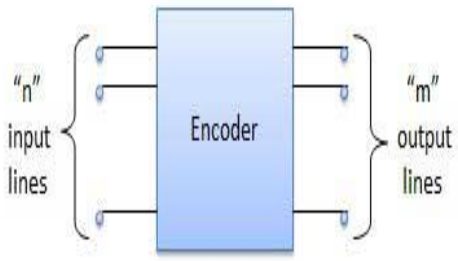

Figure 1 block diagram of encoder

Decoder: A decoder is a device which does the reverse operation of encoder, undoing the encoding so that the original information can be retrieved.

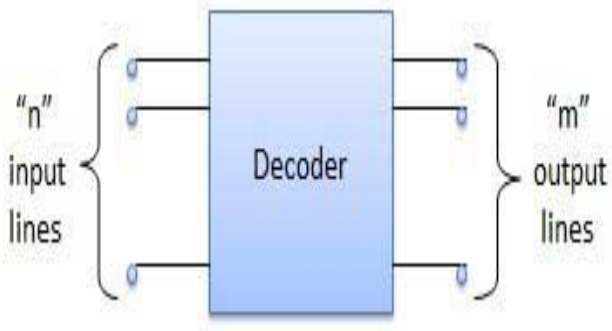

Figure 2 block diagram of decoder

A decoder that contains enable inputs is also known as a decoder-demultiplexer. Thus, we have a 4-to-16 decoder produced by adding a 4th input shared among both decoders, producing 16 outputs.

Viterbi decoding of convolution codes:

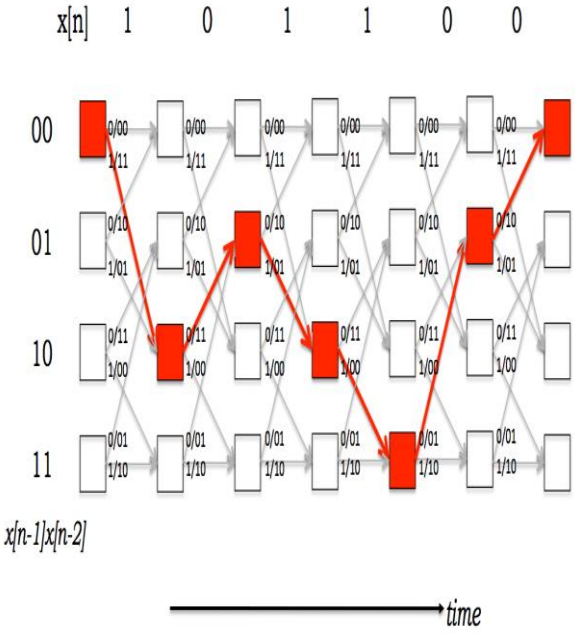

Figure 3 The trellis is a convenient way of viewing the decoding task and understanding the time evolution of the state machine

The Viterbi decoder:

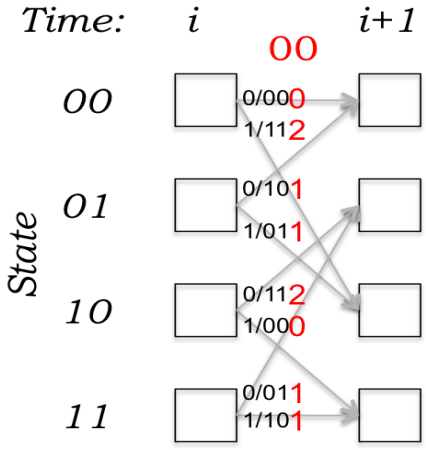

Figure 4 The branch metric for hard decision decoding, in this example, the receiver gets the parity bits 00.

III. CONCLUSION:

It is find the Viterbi decoding algorithm is mature error correct system, which will give us a BER at 8.6E-007 at 5db on an AWGN channel with BPSK modulation. By puncturing, for rate 2/3, we will pay around a 2db cost. For rate 3/4, we will pay for a 3 db cost during the transmission.

From the results, we find the Viterbi decoding algorithm is mature error correct system, which will give us a BER at 8.6E-007 at 5db on an AWGN channel with BPSK modulation. By puncturing, for rate 2/3, we will pay around a 2db cost. For rate 3/4, we will pay for a 3 db cost during the transmission. For the time issue, we do not implement a higher performance Viterbi decoder with such as pipelining or interleaving. So in the future, with Pipeline or interleave the ACS and the trace-back and output decode block, we can make it better.

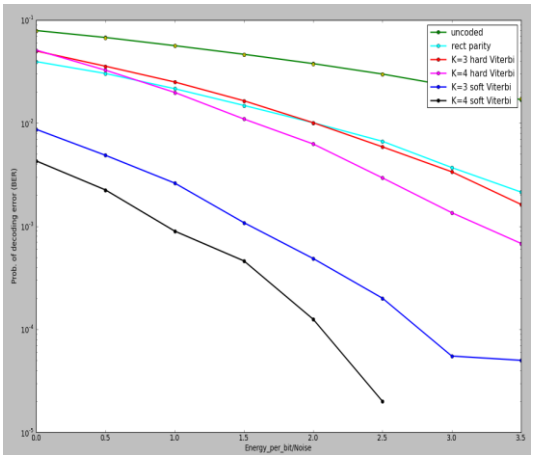

Figure 5: The comparison of different bit rate encoder performance

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