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An improved Recycling Nested Miller Compensation Amplifier with High Gain-Bandwidth

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***Abstract*— During the past decades, multi-stage amplifiers have been studied and designed to achieve better performance. According to contemporary circuit topologies, the traditional multi-stage amplifier can only achieve low gain-bandwidth (< 5 MHz) and a low slew rate (< 10 V/μs). In this paper, an improved recycling nested Miller compensation (IRNMC) amplifier is presented. By applying recycling folded cascode topology as the first stage amplifier, the proposed IRNMC amplifier improved the performance of gain-bandwidth and slew rate over that of the current multi-stage amplifiers. The proposed IRNMC amplifier is implemented in the TSMC 0.18-μm CMOS process, and is simulated using a 1.8 V power supply with a load capacitor of 100 pF. Simulation results show that the proposed IRNMC amplifier achieved a 137dB DC gain, a 15 MHz gain-bandwidth, a 62° phase margin and a 14.6 V/μs slew rate.**

***Index Terms*— Multi-stage amplifiers, recycling folded cascode topology, improved recycling nested Miller compensation (IRNMC), gain-bandwidth, slew rate.**

I. INTRODUCTION

Modern analogy amplifier circuit design and applications have indicated an increased demand on low-voltage, high-gain, high bandwidth capabilities. To achieve these goals, multi-stage amplifiers have been studied and designed to achieve better performance [1-9]. According to the proposed circuit topologies, the multi-stage amplifiers can only achieve a low gain-bandwidth (GBW) (< 5 MHz) and low slew rate (< 10 V/μs). Moreover, with the reduced size of devices, in particular the deep submicron technology process, low supply voltage requires the further reduction of the voltage gain and output swing. Thus, it is necessary to add more stages in the multi-stage amplifier design to solve this issue.

Recently, a recycling folded cascode (RFC) amplifier has been proposed to enhance the performance of traditional folded cascode (FC) amplifiers [10, 11]. The RFC amplifier can achieve a high gain and reasonably large signal swing with low voltage CMOS processes. Hence, the RFC amplifier has been employed in many applications [12].

In this paper, an improved recycling nested Miller compensation (IRNMC) amplifier has been proposed to improve the performance of the GBW and slew rate over that of current multi-stage amplifiers. The IRNMC amplifier modified the RFC amplifier by applying the nested Miller compensation (NMC) technique. To reduce complexity, the proposed amplifier applied a simple NMC technique to improve its general performance. Moreover, adding to the number of gain stages will increase the circuit's complexity. Thus, to maintain a good compromise of voltage gain and stability, frequency compensation techniques for multi-stage amplifier designs are adequate for practical purposes.

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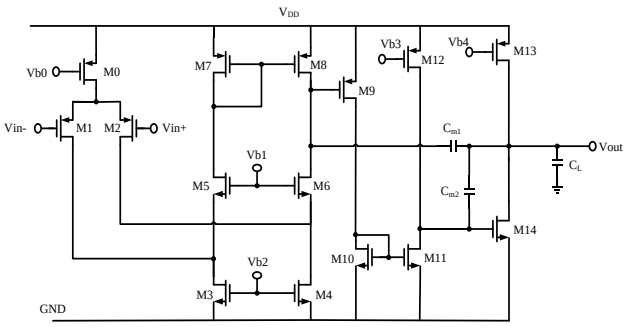

Fig. 1. The conventional nested Miller compensation (NMC) amplifier.

II. PROPOSED IRNMC AMPLIFIER

A conventional nested Miller compensation (NMC) amplifier is shown in Fig. 1. The first stage is implemented using an FC amplifier with transistors M0~M8. The transistors M3 and M4 conduct the most current; thus, they have the largest transconductance. However, the function of these transistors is limited to providing a folding node for the small signal current generated by the input drivers M1 and M2 [10]. Transistors M9~M12 realize the second gain stage. The third gain stage is the output stage with the capacitor load, and is formed by M13 and M14.

To improve on the inefficiency of conventional NMC amplifiers, an improved recycling nested Miller compensation (IRNMC) amplifier is presented in Fig. 2. In the proposed amplifier, the first stage is realized based on an RFC amplifier. The input drivers M1 and M2 (Fig. 1), are split in half to produce transistors M1, M2, M3 and M4 (Fig. 2). Next, M3 and M4 (Fig. 1) are split to form the current mirrors M7:M8 and M10:M9 with a ratio of K:1 (Fig. 2). The

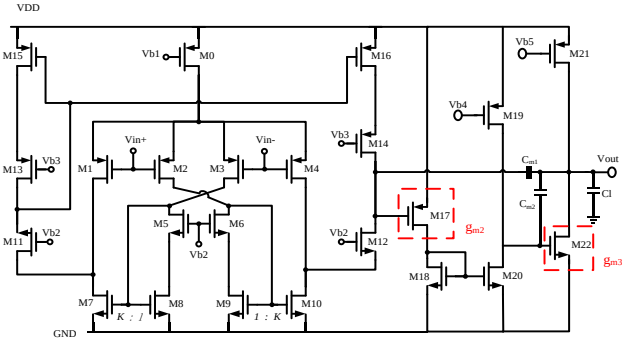

Fig. 2. Improved recycling nested Miller compensation (IRNMC) amplifier.

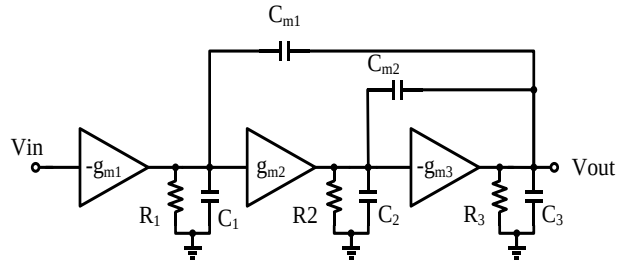

Fig. 3. Signal representation model of IRNMC amplifier.

structure of the cross-over connections from these current mirrors ensures that the currents added at the sources of M11 and M12 are in phase. To improve the matching, the size of transistors M5 and M6 are tuned to be similar to the size of M11 and M12 so that their addition helps to equally maintain the drain potentials of M7:M8 and M10:M9.

The signal representation model with the equivalent circuit of the IRNMC amplifier is shown in Fig. 3. In the figure, g_{m1}~g_{m3}, R_1~R_3, C_1~C_3 and C_L are the transconductance, output resistance, parasitic capacitance, and load capacitor, respectively. To achieve simplicity and performance at the same time, the NMC compensation technique is applied in the proposed IRNMC amplifier. The NMC compensation technique is achieved by using the Miller capacitors, C_{m1} and C_{m2}. Although many techniques have been applied in multi-stage amplifiers to achieve better performance, these compensation techniques also increased the circuit complexity [1, 2, 3, 4, 5, 6, 7, 8, 9]. Among all proposed topologies, NMC is a simple technique to stabilize multi-stage amplifiers and it can achieve general improvement for operational amplifier design [3]. Thus, to achieve simplicity and performance at the same time, NMC compensation technique is applied in the proposed amplifier.

The three-stage IRNMC amplifier can ensure a high dc gain since it is implemented by a first-stage RFC amplifier. In Fig. 3, the transconductance of the first stage amplifier, g_{m1}, and the output resistance, R_1, is represented by (1) and (2) [10].

$$g_{m1} = g_{m1a}(1+K) \quad (1)$$

$$R_1 \cong g_{m6}r_{ds6}(r_{ds2a} \parallel r_{ds4a}) \parallel g_{m8}r_{ds8}r_{ds10} \quad (2)$$

Therefore, enhancing the proposed amplifier leads to larger non-dominant poles and phase margin degeneration. From the small-signal analysis, the expression of the loop transfer function (3) is given by:

$$A_{V(\mathrm{IRNMC})} = \frac{g_{m1}g_{m2}g_{m3}R_1R_2R_3}{\left(1+\frac{s}{(C_{m1}g_{m2}g_{m3}R_1R_2R_3)-1}\right)\left(1+s\frac{C_{m2}}{g_{m2}}+s^2\frac{C_LC_{m2}}{g_{m2}g_{m3}}\right)} \quad (3)$$

The amplifier with the unity-gain feedback architecture has a third-order Butterworth frequency response [3]. The dimension of compensation capacitors can be approximated as

$$C_{m1} = 4\left(\frac{g_{m1}}{g_{m3}}\right)C_L \quad (4)$$

$$C_{m2} = 2\left(\frac{g_{m2}}{g_{m3}}\right)C_L \quad (5)$$

From (4) and (5), by decreasing the value of g_{m3}, the C_{m1} and C_{m2} can be decreased. The GBW is derived as

$$\mathrm{GBW} = \frac{g_{m1}}{C_{m1}} \quad (6)$$

From (6), by decreasing the C_{m1}, the GBW can also be enhanced. From the above discussions, we find that the first stage of the proposed RFC amplifier delivers appreciably enhanced performance over that of the traditional FC amplifier. Therefore, the proposed IRNMC amplifier can achieve better performance in relation to dc gain, GBW and slew rate.

III. Simulation Results

The presented IRNMC amplifier is designed and simulated in a TSMC 0.18μm 1P6M CMOS process, and simulated with a 1.8 V power supply, 100 pF capacitor load and compensation capacitors (C_{m1}=5pF, C_{m2}=0.12pF). In order to investigate the feasibility of the proposed IRNMC amplifier, the simulated frequency response of the proposed amplifier is compared to that of a conventional NMC amplifier. Fig. 4 shows the open loop AC response of the IRNMC amplifier. The dc gains of the NMC and IRNMC amplifiers were 66 dB and 137 dB, respectively. The NMC amplifier has a GBW of 4.19 MHz with a phase margin of 57°. The GBW of the IRNMC amplifier is 15.05 MHz, with a phase margin of 62°. The GBW and slew rate of the proposed amplifier increased due to the enhancement of gm1. The simulation results of the study show that the proposed amplifier significantly improved the performance of the GBW and slew rate over that of the NMC amplifier

For slew rate measurements, the NMC and IRNMC amplifiers are simulated when both amplifiers are loaded with a 100pF//1kΩ load. The simulated transient responses to the 500mVpp step input are shown in Fig. 5. As seen, the IRNMC amplifier clearly improved the slew rate of the NMC amplifier. The average slew rates of the IRNMC and NMC were 14.6 V/μs and 7.16 V/μs, respectively. The performance comparisons of IRNMC amplifiers and reported multi-stage amplifiers are summarized in Table I. It can be observed that the IRNMC achieved a 259% improvement in GBW compared to the NMC. For the average slew rate, the IRNMC achieved a 104% improvement compared to the NMC.

Moreover, the reported multi-stage amplifiers achieved a low slew rate (< 5 V/μs) and low GBW (< 5 MHz). However,

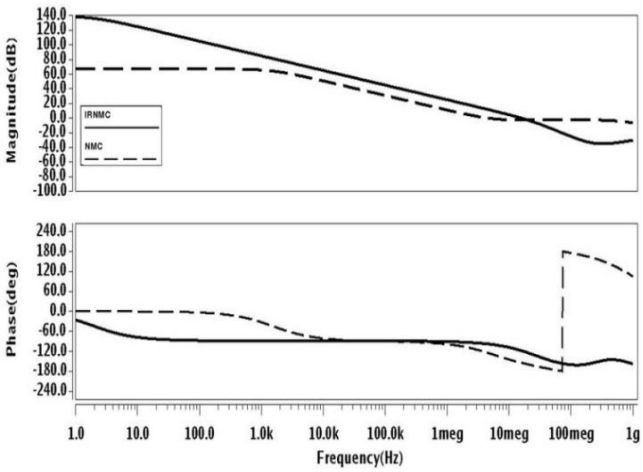

Fig. 4. Simulated open loop AC responses of IRNMC and NMC amplifiers.

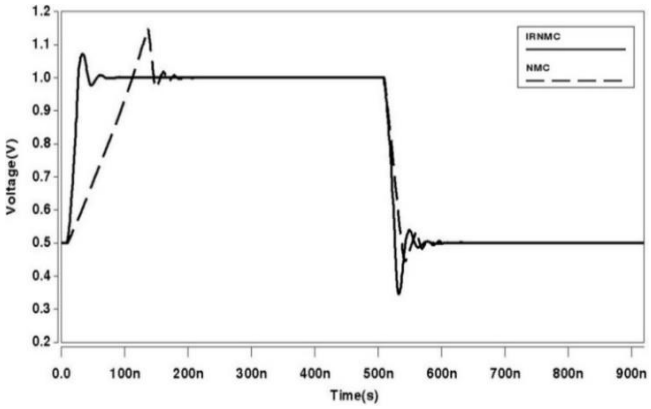

Fig. 5. Transient responses of amplifiers with a 100pF//1kΩ load.

Table 1. Performance summary of different multi-stage amplifiers

Parameter	This work (IRNMC)	This work (NMC)	[7]	[8]	[9]
Technology (μm)	0.18	0.6	0.35	0.065	0.18
C_L (pF)	100	100	500	500	250
DC Gain (dB)	137	66	>100	>100	>100
Phase margin (deg)	62	57	70	52	73
GBW (MHz)	15.05	4.19	4	2	4.4
Slew Rate (V/μs)	14.6	7.16	2.23	0.65	1.8

the proposed IRNMC amplifier can achieve a 14.6 V/μs slew rate and 15 MHz GBW. Obviously, the IRNMC amplifier significantly improved the performance of the average slew rate and GBW over that of other reported multi-stage amplifiers with compensation topologies.

IV. Conclusion

An improved recycling nested Miller compensation (IRNMC) amplifier was proposed herein to improve the general performance of reported multistage amplifiers via a compensation technique. By modifying the RFC amplifier using the nested Miller compensation (NMC) technique, the proposed amplifier significantly enhanced the performance of the DC gain, gain-bandwidth and slew rate over the NMC amplifier. The simulation results show that the gain-bandwidth and slew rate were enhanced by 259% and 104% over that of the NMC amplifier.

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