Investigation on Control Strategies of Multilevel Inverter for Improved Power Quality

Rupali Choukesey, Kaushal Sengar, E Vijay Kumar

Abstract— Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. This paper presents the most important topologies like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multicell with separate dc sources. Emerging topologies like asymmetric hybrid cells and soft-switched multilevel inverters are also discussed. This paper also presents the most relevant control and modulation methods developed for this family of converters: multilevel sinusoidal pulse width modulation, multilevel selective

harmonic elimination, and space-vector modulation. Special attention is dedicated to the latest and more relevant applications of these converters such as laminators, conveyor belts, and unified power-flow controllers. The need of an active front end at the

input side for those inverters supplying regenerative loads is also discussed, and the circuit topology options are also presented. Finally, the peripherally developing areas such as high-voltage high-power devices and optical sensors and other opportunities for future development are addressed. MATLAB simulation

Index Terms—Power Quality, THD, MATLAB/Simulink.

I. INTRODUCTION

IN RECENT YEARS, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids (2.3, 3.3, 4.16, or 6.9 kV). For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels [1]-[3]. inverters include an array Multilevel of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages.

II. POWER QUALITY

Power quality determines the fitness of electrical power to consumer devices. Synchronization of the voltage frequency and phase allows electrical systems to function in

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their intended manner without significant loss of performance or life. The term is used to describe electric power that drives an electrical load and the load's ability to function properly. Without the proper power, an electrical device (or load) may malfunction, fail prematurely or not operate at all. There are many ways in which electric power can be of poor quality and many more causes of such poor quality power.

The electric power industry comprises Electricity Generation (AC power), electric power transmission And ultimately electricity distribution to an electricity meter located at the premises of the end user of the electric power. The electricity then moves through the wiring system of the end user until it reaches the load. The complexity of the system to move electric energy from the point of production to the point of consumption combined with variations in weather, generation, demand and other factors provide many opportunities for the quality of supply to be compromised. While "power quality" is a convenient term for many, it is the quality of the voltage rather than power or electric current that is actually described by the term. Power is simply the flow of energy and the current demanded by a load is largely uncontrollable.

III. BACKGROUND OF THE RESEARCH

Multilevel inverters have been under research and development for more than three decades and have found successful industrial applications. However, this is still a technology under development, and many new contributions and new commercial topologies have been reported in the last few years. The aim of this dissertation is to group and review recent contributions, in order to establish the current state of the art and trends of the technology to provide readers with a comprehensive and insightful review of where multilevel converter technology stands and is heading. This chapter first presents a brief overview of well-established multilevel inverters strongly oriented to their current state in industrial applications and then centres the discussion on the new multilevel inverters that have made their way into the industry. Multilevel inverters have been attracting increasing interest recently the main reasons are; increased power ratings, improved harmonic performance, and reduced electromagnetic interference (EMI) emission that can be archived with multiple DC levels that are synthesis of the output voltage waveform. In particular multilevel inverters have abundant demand in applications such as medium voltage industrial drives, electric vehicles, and grid connected photovoltaic systems. The present work provides a solution to design an efficient multilevel topology which is suited for medium and high power applications. In the subsequent sections the research background is discussed in detailed. Motivation and objectives are clearly outlined.

Multilevel converters are power-conversion systems composed by an array of power semiconductors and

capacitive voltage sources that, when properly connected and controlled, can generate a multiple-step voltage wave form with variable and controllable frequency, phase, and amplitude. The stepped waveform is synthesized by selecting different voltage levels generated by the proper connection of the load to the different capacitive voltage sources. This connection is performed by the proper switching of the power semiconductors [14, 15, and 59].

The inverter is an integral component of the power conditioning unit of a photovoltaic power system and employs various DC /AC converter topologies and control structure. It has to meet various international standards before it can be put in commercial use. The function of inverter in distributed power generation system on top of photovoltaic generation includes DC -AC conversion, output power quality assurance, various protection mechanisms, and system controls. The requirements in terms of low cost, high efficiency, high reliability, and tolerance over wide range of input voltage variations have driven the inverter development toward simpler topologies, lower component counts, and tighter modular design. Historically, the inverters employed in PV technology may be classified based on number of power processing stages, type of power decoupling, types of interconnection between the stages, and types of grid interface. Based on power processing stage, the inverter may be classified as single stage and multiple stage inverters. This paper presents a comprehensive review of various inverter topologies and control structure employed in PV applications with associated merits and demerits. The paper also gives the recent trends in the development of PV applications [4, 61, 62 and 65].

IV. PURPOSES/OBJECTIVES OF THE RESEARCH

In this dissertation work, I am investigating the Various Pulse Width Modulations (PWM) Control Strategies for Multilevel Inverter (MLI) Topology on the basis of following aspects:

- Power Quality Enhancement Capabilities.
- Compare the most popular Sinusoidal Pulse Width Modulation (SPWM) Techniques on Three-Level and Five-Level MLI through MATLAB/SIMULATION.
- Compare the Power Quality of Output Voltage Waveform for Total Harmonic Distortion (THD) for Different PWM Schemes.

Analyze the results of modulation schemes by various carrier frequency, modulation index and modulation schemes

V. PROBLEM SPECIFICATIONS

When output of sinusoidal PWM model are provided to 3-level and 5-level waveforms for single phase and three phase also. Then the THD is different from all the schemes and we are compare harmonics for all the waveforms. The Diode Clamped Multilevel Inverter deals with a brief overview of different topologies and new research topics in this field are presented and their advantages and disadvantages are discussed briefly. In addition, these topologies are compared in different aspects. At the end, the different modulation schemes are compared of Diode Clamped multilevel inverter discussed. Focus is made on the carrier based PWM methods wherein the PWM methods based on both the variation of carrier signal and variation of reference signal are discussed. These methods are then compared in terms of overall THD and the presence of lower order harmonics.

Focus is made on a 5-level topology whose different working modes and output voltage and current equations are derived. A suitable control scheme is derived for the control of the proposed topology. Based on this, the three-phase system is also derived wherein the major focus is kept on the control part. Comparison is made with classical multilevel inverter topologies for both single-phase and three-phase applications. Simulation results for а 5-level switched-capacitors inverter for both single-phase and three-phase systems. A nine-level switched-capacitors inverter with PV array as a source is also simulated to show the compatibility of the proposed configuration with renewable energy sources.

VI. BRIEF TECHNOLOGY/METHODOLOGY OF THE RESEARCH

Multilevel inverters utilize an array of power switches and several lower voltage DC sources to generate a stepped output voltage waveform with variable and controllable frequency, phase and amplitude. Batteries, capacitors and renewable energy resources can be used as multiple DC voltage sources. Figure 1.2 shows one phase leg of multilevel inverters. In this schematic diagram, operations of semiconductors are shown by an ideal switch with several states. Adopted switching scheme is such that the operation of switches and their commutation allows the addition of the multiple DC voltage sources to generate high voltage at the output while the power switches must withstand only reduced voltages.

To be called a multilevel inverter, the power circuit has to generate at least three different voltage levels at the output. These voltage levels follow an inverse relation with the harmonic content in the output i.e. more the number of levels, better will be the harmonic profile of the output. Thus by increasing the output voltage levels, harmonic content of the waveform can be reduced to minimum, since the waveform will be close to a sinusoid. However, in practice the Accessible voltage levels are governed by factors like voltage unbalancing problems and power losses [3]. In this paper, first the structure of the inverter is explained and then the conventional multilevel inverter topologies are discussed with their relative advantages and disadvantage over each other. Both the symmetric and asymmetric configurations are covered under this category.

VII. BENEFITS AND EXPECTED OUTCOMES OF THE RESEARCH

The elementary concept of multilevel inverter involves the Power Quality Enhancement Capabilities. Compare the most popular Sinusoidal Pulse Width Modulation (SPWM) Techniques on Three-Level AND Five-Level MLI through MATLAB/SIMULATION. Compare the Power Quality of Output Voltage Waveform for Total Harmonic Distortion (THD) for Different PWM Schemes. Analyse the results of modulation

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Figure 1. One phase leg of a multilevel inverter

In this schemes by various carrier frequency, modulation index and schemes by various carrier frequency, modulation index and modulation schemes. Multilevel inverters can be mainly divided into three major groups:

- Diode-clamped multilevel inverter (DCMLI)
- Flying capacitors multilevel inverter (FCMLI)
- Cascaded H-bridge multilevel inverter (CHBMLI)

Multilevel inverters have a number of advantages over the conventional two-level high switching frequency PWM inverter Some of these are listed below.

- Improved Harmonic profile of output.
- Reduced size of output filter
- Low dv/dt stress
- Ability to operate at both low and high switching frequency
- Modular architecture
- Possibility of fault tolerant operation
- Reduced EMI and common mode voltage
- Renewable energy resources in the form of Photovoltaic (PV), Wind Turbine (WT) and Fuel-Cell can be interfaced easily as DC voltage sources.

In this research we are expected more power quality using different modulation schemes, reduces harmonics and we are change input waveforms (e.g. saw tooth, triangular) then getting different output sinusoidal waveforms with minimum harmonics. To day, multilevel inverters have found wide area of applications, specifically high power medium voltage drives, HVDC transmission, distributed generation, static var compensation, electric vehicular technology, and grid connected renewable energy systems and many more. In fact, some researchers are suggesting their employment even for low power applications (e.g. aircraft systems) [13, 14].

VIII. ANALYSIS OF RESULTS

In this research area we are investigate the nine different modulation schemes of Diode Clamped Multilevel Inverter. We are analysing the difference of THD in all the schemes of line voltage and phase voltage and clearly shown by table .1 and .2.

The first experimentation is carried out to investigate the performance of three-phase, five-level diode clamped multilevel inverter SPWM control validate the simulation results with Sinusoidal PWM schemes. Further the inverter is tested with PD SPWM, VAPD SPWM, POD SPWM, VAPOD SPWM, APOD SPWM, VAAPOD SPWM, VF SPWM, CO SPWM – A, CO SPWM –B and their modified forms with addition of off-set signal. It indicates the unequal voltage stresses on the devices in the same phase leg of inverter. Inverter line voltages with PD SPWM scheme, POD SPWM scheme, PD with off-set signal and POD SPWM with off-set signal technique. The frequency spectrum of line voltage Vab with these different SPWM schemes are discussed in last chapter. The lowest harmonic distortion is 16.97%. Line voltage contains increased magnitude of harmonics around the switching frequency and THD contents are 20.08 % in POD SPWM and POD SPWM with off-set signal respectively.

Figure 2 shows the three-phase output line voltage with five level diode clamped multilevel inverter SPWM technique at amplitude is 400 volts and switching frequency is 4 KHz.



Figure 2 Line voltages of the proposed three-phase inverter



Figure 3 Phase voltages of the proposed three-phase inverter

Figure .3 Shows the three-phase output voltage with five level diode clamped multilevel inverter SPWM technique at amplitude is 400 volts and switching frequency is 4 KHz. Figure 2 Phase voltages of the proposed three-phase inverter

Table 1 and 2 compare the performance of DCMLI with different SPWM schemes on no-load and on-load conditions on the basis of %THD, amount of DC link unbalance and fundamental voltage output. The THD content in inverter voltage in minimum in PD SPWM investigation in chapter 4. This schemes also gives minimum DC link unbalance without using any controller. It is clear that phase voltage contains 3rd order harmonic due to inherent problem of capacitor voltage unbalancing. These results confirm the correctness of the developed inverter and its controller experimentally. The best techniques in my research work is PDPWM which has been provide minimum harmonics 16.95% and APOPWM techniques has maximum 25.15% harmonics.

The valuable data of bar frequency we are showing here FFT calculation and we getting to compare maximum harmonics in all that schemes order with sinusoidal waveform and her frequency analysis tool and maximum harmonic of 81 i.e. 9.06% and value of frequency is 4050 Hz.

FFT analysis-							
	Sampling ti	me = 5e-	006 s				
	Samples per	cycle = 400	0				Ê.
	DC componer	nt = 0.0	4726				
	Fundamental	= 210	.4 peak (14	B.B rms)			
	Total Harmo	onic Distorti	on (THD) =	23.80%			
	2 3 4	1.2					
	hax 1000 hat	monic freque	ncy	00 11- /10	Cosh hammaist		
	used for	nD calculati	on - 99900	.UU HZ (19	95th narmonic)		
	0 Hz	(DC):	0.02%	270.0°			
	25 Hz	1201.	0.01%	-86.5°			
	50 Hz	(Fnd):	100.00%	-0.1°			
	75 Hz	(1.111)	0.01%	51.2°			
	100 Hz	(h2):	6.06%	269.8°			
	125 Hz	6.35	0.00%	174.0°			
	150 Hz	(h3):	0.13%	-21.2°			
	175 Hz		0.00%	214.1°			
	200 Hz	(h4):	2.16%	268.9°			
	225 Hz		0.00%	233.1°			
	250 Hz	(h5):	1.51%	180.4°			
	275 Hz		0.00%	115.1°			
	300 Hz	(h6):	0.00%	139.6°			*
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	F1	gure 4	FFI	data	for Har	monics ord	er
T analysis-							
	205.0	- (1-77) -		0.104	10.20		
	3030 1	12 (11/7):		0.128	100.0		^
	2000 1	14		0.00%	145.0		
	3900 5	12 (11/8):		0.00%	193.0		
	3925 8	1Z		0.00%	103.0		
	3950 B	iz (n/9):		8.9/%	63.3		
	39/5 8	12		0.00%	-23.3		
	4000 1	Hz (h8U):		U.U5%	48.9		
	4025 1	iz		U.UU%	-12.6		-

1000 112 (1100/.	0.000	10.0	
4025 Hz	0.00%	-12.6°	
4050 Hz (h81):	9.06%	243.4°	
 4075 Hz	0.00%	139.0°	
4100 Hz (h82):	0.88%	149.1°	
4125 Hz	0.00%	203.5°	
4150 Hz (h83):	0.06%	213.5°	
4175 Hz	0.00%	151.1°	
4200 Hz (h84):	3.01%	154.7°	
4225 Hz	0.01%	148.6°	
4250 Hz (h85):	4.41%	-31.0°	
4275 Hz	0.00%	-65.9°	*

Figure 5 Fundamental frequency bar with maximum harmonic

Table .1 Fundamental Frequency and %THD of line voltage for Different Modulation Indices for Conventional PWM Strategy

Different Modulation schemes	Fundamental frequency - line voltage	Total harmonic distortion (THD) - line voltage
PDPWM	348.1	16.95
VAPDPWM	377.0	17.39
PODPWM	377.0	20.16
VAPODPWM	367.1	20.15
APODPWM	346.9	25.15
VAAPODPWM	376.9	21.23
VFPWM	346.8	18.78
COPWM-A	364.1	21.21
COPWM-B	364.1	23.87

It is clear from table 6.1 and 6.2 that within one fundamental frequency for line voltage and phase voltage and total harmonic distortion for line and phase voltage for different

modulation schemes. The fundamental cycle of inverter output, inner switches remain conducting for large duration as compared to outer switches in 3-level and 5-level inverter resulting in unequal conduction duty ratios of each switching device. Therefore, it is important to measure voltage and current across each switch as their conduction intervals and voltage are not equal.

Table . 2 Fundamental Frequency and %THD of phase voltage for Different Modulation Indices for Conventional PWM Strategy

Different Modulation schemes	Fundamental frequency- phase voltage	Total harmonic distortion(THD) - phase voltage
PDPWM	201.3	16.97
VAPDPWM	217.7	17.42
PODPWM	217.7	20.08
VAPODPWM	216.1	20.04
APODPWM	200.3	25.13
VAAPODPWM	217.7	21.09
s VFPWM	200.3	18.76
COPWM-A	210.3	21.21
COPWM-B	210.4	23.80

IX. CONCLUSION

Recent development in this technology enable to achieve high efficiency, energy savings, improved performance, and compactness in almost all domestic, commercial, industrial and utility based applications. The solution of this power quality problem again employ improved performance converters. Pulse width modulation converter have become an integral part of these improved performance converters, require high voltage, high frequency switching devices. Recently multilevel inverters are being emerged as a viable solution of conventional 2-level inverter for medium and high voltage applications with improved power quality. In this dissertation a single phase five level diode clamped inverter is designed, developed and investigated for improve voltage quality in terms of harmonic distortion with reduce switching losses. An exhaustive literature survey is carried out on different multilevel inverter to review the state of art of multilevel inverter technologies based on topologies, modulation schemes, and application techniques. A three-level diode clamped inverter is then investigated through simulation using different multilevel modulation schemes such as sinusoidal pulse width modulation (SPWM). An improved performance of the inverter is obtained with SPWM and their modified forms (PD SPWM, VAPD SPWM, POD SPWM, VAPOD SPWM, APOD SPWM, VAAPOD SPWM, VF SPWM, CO SPWM – A, CO SPWM -B) in terms of load side power quality such as sinusoidal load voltages and current with their THD.

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