Control Strategy for Fault Current Interruption in a Radial Distribution Line using Dynamic Voltage Restorer

M. Prasanthi, Dr. D. Vijaya Kumar

***Abstract*— These days power quality is becoming increasingly essential in industrial electricity consumers point of view. This paper proposes a control strategy of DVR which interrupts fault current in a radial distribution line using dynamic voltage restorer (DVR). Under the conditions of linear and non-linear loads the DVR detects and compensates voltage sags effectively. This control scheme can interrupt fault current within few seconds. The magnitude and phase of measured voltages is estimated using digital filters which adequately mitigates the impacts of harmonics, disturbances and noise on the phasor parameters. The results of the simulation studies are performed in the MATLAB SIMULINK software. For this control scheme, phase locked loop is not required so that for each phase, the injected voltages of which magnitude and phase angle can be controlled independently. By using Matlab/Simulink software, these simulation studies give results: 1) Under different fault conditions, the proposed control system performs satisfactorily. 2) The point of common coupling voltage is also restored by using this control scheme of DVR.**

***Index Terms*— Dynamic voltage restorer (DVR), fault current interrupting, voltage sag and voltage swell.**

I. INTRODUCTION

Custom power device (CPD) is a powerful tool to protect sensitive loads if there is any disturbance from power line and it is based on semiconductor switches concept. There are many custom power devices; one such is Dynamic Voltage Restorer (DVR) which is used to prevent voltage sags [1], [2].

To enhance voltage quality, three phase ac voltages are injected in series with the supply voltage by DVR which also adjusts the wave shape, phase angle and voltage magnitude. The main components of a DVR are a series transformer, a harmonic filter, a voltage- source converter (VSC), a dc-side capacitor and an energy storage device [5], [6]) as shown in Fig. 1. The line-side harmonic filter [4] comprises of the filter capacitor and the leakage inductance of the series transformer.

To increase energy efficiency and productivity, control devices, sensitive power electronic equipments and non-linear loads are employed by modern industries as part of automated processes. Industrial systems use large number of practiced and sensitive electronic equipment which results in voltage disturbances, the most common power quality problem. DVR is a series compensation device, which is introduced recently to protect sensitive electric load from power quality problems such as voltage sags, swells, unbalance and distortion by means of power electronic controllers that use voltage source converters (VSC).

Voltage sags is defined as a sudden reduction of supply voltage from 90% to 10%of nominal with a recovery in short period of time. It is examined as the most serious problem of power quality that can occur at any time with amplitude ranging from 10%-90% for a duration lasts for half a cycle to one minute. Voltage sags is caused either by starting of large induction motor or fault in power system which can interrupt any electrical or electronic equipment that is load sensitive. There will be huge loss if the voltage sag is at customer load end.

On the other hand an increase in rms voltage or current at the power frequency is defined as voltage swell with duration ranges from 0.5 cycles to 1 min, typical magnitude is between 1.1 and 1.8 up and swells magnitude is greater than 1.0 in this case.

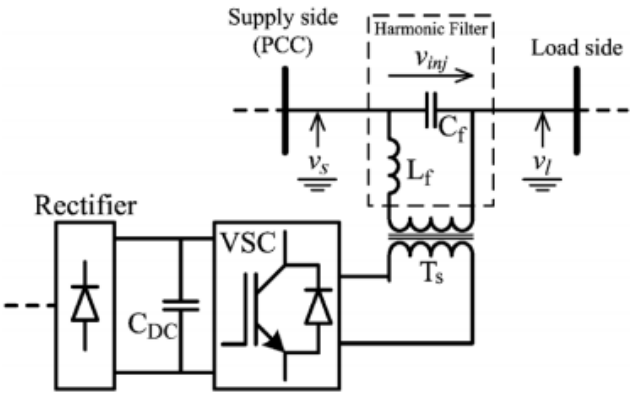

Fig. 1. Schematic diagram of a DVR with a line-side harmonic filter.

In distribution systems voltage swells are less common compared to voltage sags, thus they are of not much importance. Both voltage sag and swell can cause failure or shutdown of sensitive equipment such as found in semiconductor or chemical plants and a large current unbalance is created that could blow fuses or trip breakers. The effects ranging from minor quality variations to production downtime and for the customer the equipment damage are very expensive.

Different methods were introduced to reduce voltage sags and swells but the most efficient method is the use of

M.Prasanthi, , Dept. Electrical and Electronics Engineering, AITAM, Tekkali, India, Ph: 8179984969.

Dr.D.Vijaya Kumar, Prof., Dept. Electrical and Electronics Engineering, AITAM, Tekkali, India.

custom power device i.e., DVR. Energizing a large capacitor bank or Switching off a large inductive load causes swells.

Dynamic Voltage Restorer with its operating principle is introduced in this paper and to compensate voltage sags/swell a simple control based on DQO method is used. The simulation is done using MATLAB/SIMULINK. The simulation results validate the effectiveness of the proposed control method of DVR.

II. CONTROL STRATEGY FOR FCI

In a distribution network load side voltage is regulated by the Dynamic Voltage Restorer (DVR) which is a series connected device. The DVR provides a three phase independently controlled voltage source utilizing power electronic components, whose voltage vector (magnitude and angle) is added to the source voltage to restore the load voltage to a prescribed level. The adopted DVR converter consists of three independent H-bridge VSCs which are connected to a common dc-link capacitor. These VSCs are connected in series with the supply grid through a single phase transformer. In the proposed FCI control system there are three independent and identical controllers for each single-phase VSC of the DVR. Let us assume the fundamental frequency components supply voltage v_s, load voltage v_l, and the injected voltage v_{inj}, from Fig. 1 are

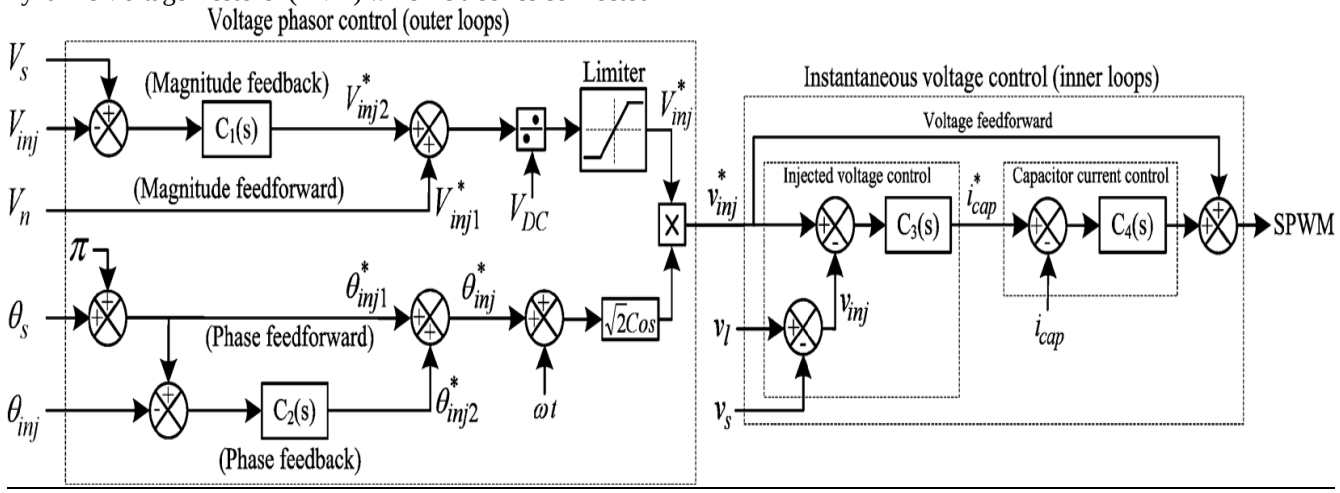

Fig. 2. Per-phase block diagram of the DVR control system in FCI mode.

$$v_s = V_s \times \cos(\omega t + \theta_s) \quad (1)$$
$$v_l = V_l \times \cos(\omega t + \theta_s) \quad (2)$$
$$v_{inj} = v_l - v_s = V_{inj} \times \cos(\omega t + \theta_{inj}) \quad (3)$$

To measure the phase angles and magnitudes of the phasors corresponding to v_s and v_{inj} (i.e., $\overrightarrow{V_s} = V_s \angle \theta_s$ and $\overrightarrow{V_{inj}} = V_{inj} \angle \theta_{inj}$, respectively in 5 ms [5], two identical least error squares (LES) filters [9] are used. Per-phase block diagram of the proposed DVR control system corresponding to the FCI operation mode is shown in Fig. 2, where V_n is the nominal RMS phase voltage. The over current fault detection method of [5] and [8] gives the recorded studies in this paper. When the absolute value of the instantaneous current exceeds double the rated load current then the fault detection mechanism is activated for each phase. The proposed multi loop control system [3], [6], [10]–[12] includes an outer control loop (voltage phasor control) and an inner control loop (instantaneous voltage control). The DVR harmonic filter causes the transients for which the inner loop provides damping [11] and [13], and improves the dynamic response and stability of the DVR. The sag compensation and the FCI functions share the inner loop. The injected voltage magnitude and phase angle of the fault phase is controlled by the outer loop when a downstream fault is detected, which also reduces the load-side voltage to zero in order to interrupt the fault current and restore the PCC

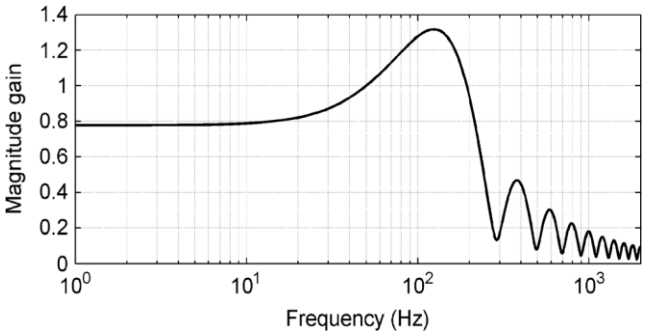

Fig. 3. Magnitude of the LES filters frequency response.

voltage. The following two subsections describes the DVR "outer" voltage phasor control and "inner" instantaneous voltage control corresponding to each phase.

A. Voltage Phasor Control System

The injected voltage phasor which is required is equal to source voltage phasor in this FCI operation mode, but in phase opposition [i.e., the injected phasor $\overrightarrow{V_{inj}} = V_{inj} \angle \theta_{inj}$ is controlled to be $V_s \angle (\theta_s + \pi)$]. Hence in terms of transient response, speed, and steady-state error, the performance of the voltage phasor control is improved by controlling voltage magnitude and phase separately. And the feed forward signals are included to feedback control system [7], [8], [10] – [13]. From Fig. 2 we can observe that the two proportional-integral (PI) controllers (C_1 and C_2) can be used for removing the steady-state errors of the magnitude and phase of the injected

voltage. Hence with zero steady state error the parameters of each controller are regulated for attaining fast response.
So, the output of the phasor control system is a reference phasor that can be represented as $\overrightarrow{V_{inj}^{*}} = V_{inj}^{*}\angle\theta_{inj}^{*}$. So, V_{inj}^{*} is regularized by V_{dc} to terminate the effects of the dc-link voltage variations on the injected voltages. The magnitude and the phase angle of V_{inj}^{*} are calculated separately. Then the magnitude is passed through a limiter in voltage phasor control (Fig. 2). The phasor magnitude and phase angle which are ensued are converted to the sinusoidal signal. This is the reference signal for the instantaneous voltage control.

B. Instantaneous Voltage-Control System

Under ideal conditions, if output of the phasor-based controller V_{inj}^{*} is fed instantaneously to the sinusoidal pulse-width modulation (SPWM) unit a voltage sag can be compensated successfully. However, even under these conditions the resonances of the harmonic filter cannot be removed effectively. Hence, to enhance the stability and dynamic response of the DVR, an instantaneous injected voltage controller and a harmonic filter capacitor current controller are used for attenuating resonances.

The reference signal which is generated for the injected voltage v_{inj}^{*} is then compared with the measured injected voltage v_{inj}. Also the error which is obtained is fed to the voltage controller. From Fig. 2, we observe that the output of the voltage controller i_{cap}^{*} is the reference signal for the filter capacitor current control loop and again it is compared with the measured capacitor current i_{cap}. Then the error is fed to the current controller. From the proposed control system, the steady-state error is completely eliminated in the outer control loop (say C_1 and C_2) by means of PI controllers. Through this the dc signals (magnitude and phase angle) are tracked. Consequently, in the inner control loop the higher order controllers are not required as these are designed depending on sinusoidal references. Thus, from Fig. 2, we can see that C_3 and C_4 are pure gains k_v and k_c respectively. The k_v when large cause the DVR filter resonance which can be amplified so that the stability of the system is affected skeptically [12]. Hence, by a feed forward loop the transient response of the DVR is improved and the voltage controller is used as a small proportional gain. When the k_c is large, harmonic filter resonance is damped by it more effectively, which is limited by practical considerations (e.g., amplification of capacitor current noise, measurement noise, and dc offset [8]). So, the proportional gain has lowest value which damps the resonances and it is used effectively. Hence, the feed forward voltage is added to current controller output for derivation of the signal for PWM generator.

III. STUDY RESULTS

Fig 4 shows a single-line diagram of a power system for which the performance of the proposed DVR control system is judged under different fault conditions using MATLAB/ SIMULINK software environment. In this control system, 525-kVA DVR system is installed on the 0.4-kV feeder, for protecting a 500-kVA, 0.90 lagging power factor load against voltage sags. Here, the base voltage for per-unit values is the nominal phase voltage.

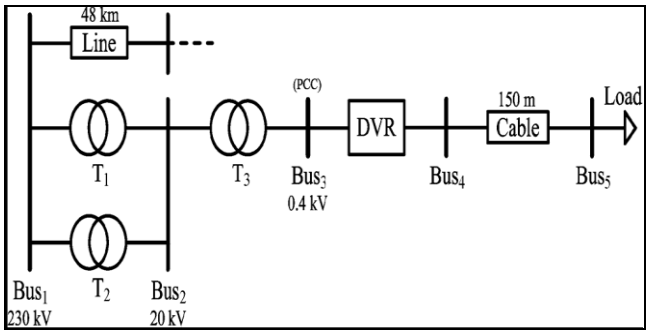

Fig. 4. Single-line diagram of the system used for simulation studies.

A. Three-Phase Downstream Fault

In Fig. 4 the Bus 3 of the system is subjected to a three phase short circuit with a negligible fault resistance at 0.15 sec prior to the fault initiation, the DVR is inactive or in standby mode. During the fault, if the DVR is bypassed, as shown in Fig. 5 the voltage at Bus3 drops about 0.3 p.u. and the fault current increases to about 20 times the rated load current.

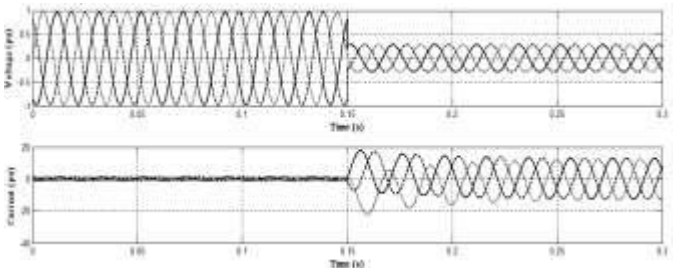

Fig. 5. (a) Voltages at Bus 3. (b) Fault currents, during downstream three phase fault when the DVR is inactive.

Using the proposed controller for DVR the same system shown in Fig. 4 is simulated. Fig. 6(a)–(b), shows the restored three-phase supply-side voltages, and the three-phase load side voltages respectively. Load voltage is reduced to zero to interrupt the fault currents. The source voltage is restored and Fig. 6(c) illustrates that the proposed FCI method limits and interrupts the maximum three-phase fault current effectively within short interval of time.

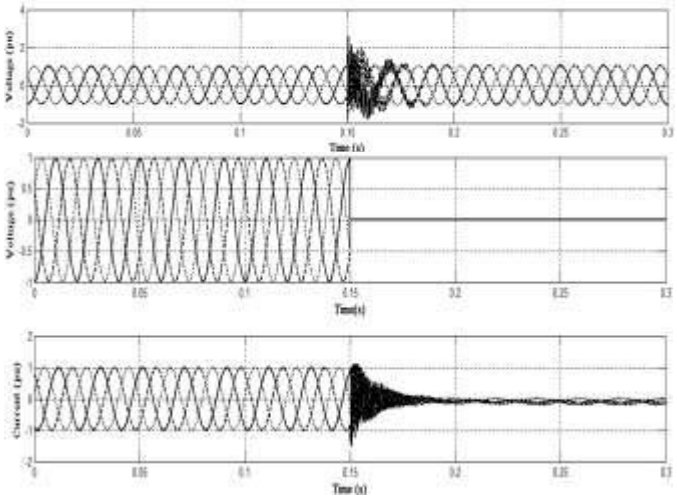

Fig. 6. (a) Source voltages. (b) Load voltages. (c) Line currents during the three-phase downstream fault

B. Line-to-line Downstream Faults

The system of Fig. 4 is subjected to a phase-A to phase-B fault with a fault resistance of 0.001.Fault is initiated at 0.15 sec. When the DVR is inactive or bypassed during the fault, as shown in Fig. 7 the PCC voltage drops to 0.6 p.u and also the fault current increases to about 13 times the rated load current. That is high fault current flow through the system.

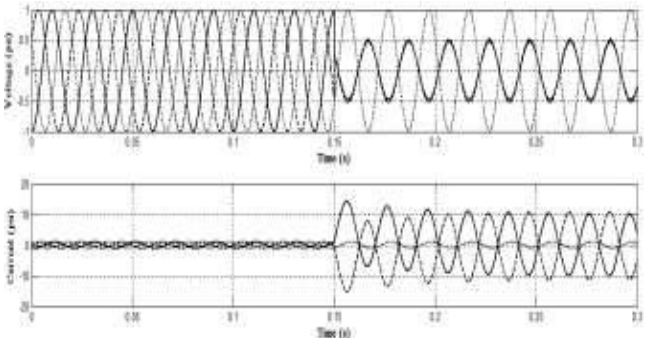

Fig. 7. (a) Voltages at Bus 3(b) Fault currents, during downstream phase-to phase fault when the DVR is inactive

Fig. 8 (a)–(b), respectively, shows the restored supply-side voltages, and the load-side voltages. Supply side voltage is restored and load side voltage is reduced to zero to interrupt the fault currents and the line currents. FCI control successfully interrupts the fault current and restores the source voltage of the faulty phases within less time. It also shows that only the two faulty phases of the DVR is affected, and the healthy phase is not interrupted.

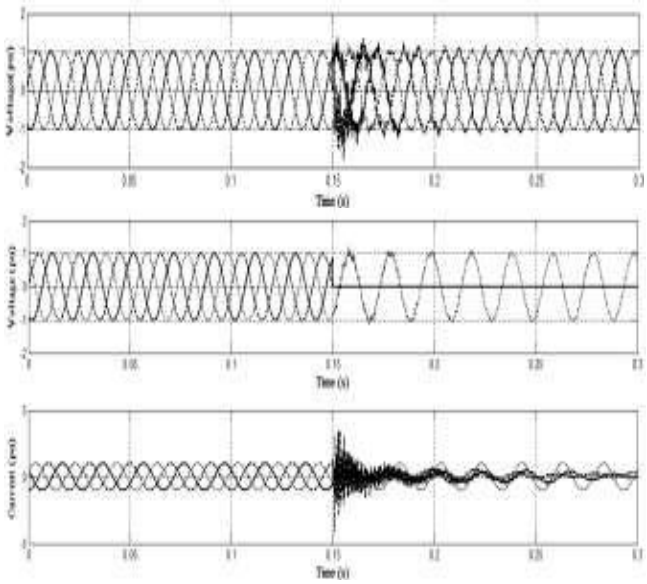

Fig. 8. (a) Source voltages. (b) Load voltages. (c) Line currents during the line-line downstream fault

C. Line-to-Ground Downstream Fault

Phase-C of the system shown in Fig. 4 is subjected to a fault with a negligible resistance of 0.001and the fault is initiated at 0.15 s. If the DVR is inactive, as the result shown in Fig.9, the voltage at PCC considerably drops to about 0.2 pu and the fault current increases 16 times rated current for the faulty phase C.

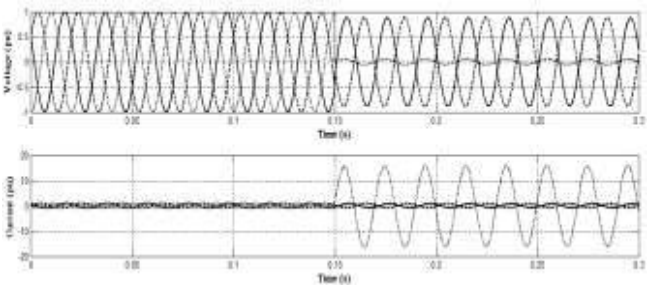

Fig. 9. (a) Voltages at Bus 3 (b) Fault currents, during the downstream single phase- to-ground fault when the DVR is inactive.

Fig. 10 (a)–(c), respectively, shows the restored supply-side voltage for the faulty phase, the load-side voltage and the interrupted fault current. Load side voltage for faulty phase are reduced to zero to interrupt the fault currents and the line currents while the healthy phase remains the same in magnitude. FCI control successfully interrupts the faulty current and restores the voltage of the faulty phases within less time. It also shows that only the faulty phase, phase C of the DVR is affected, and the healthy phases are not interrupted.

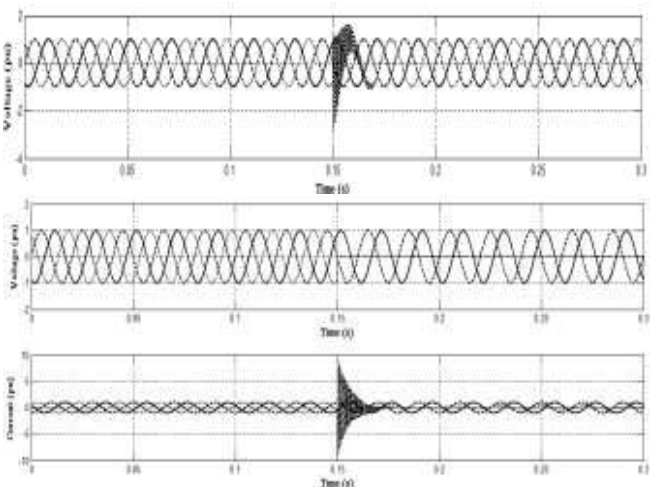

Fig. 10. (a) Source voltages. (b) Load voltages. (c) Line currents. during the single-phase-to-ground downstream fault.

IV. SIMULATION RESULTS

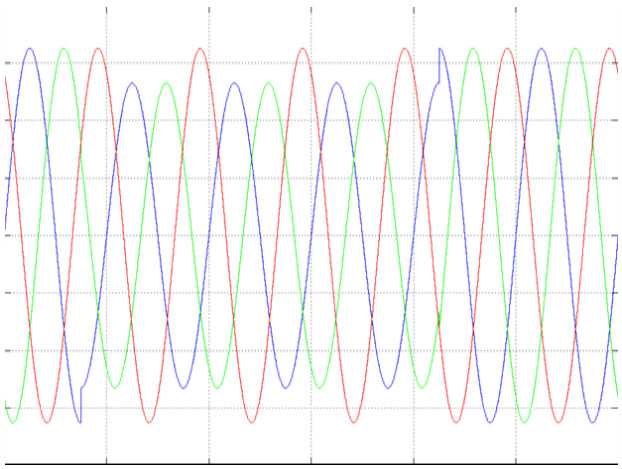

Fig. 1 Supply voltages

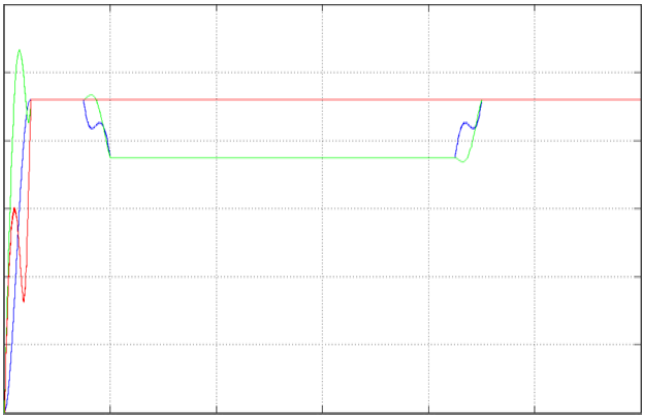

Fig. 2: Estimated supply voltage magnitude vs of depressed phases

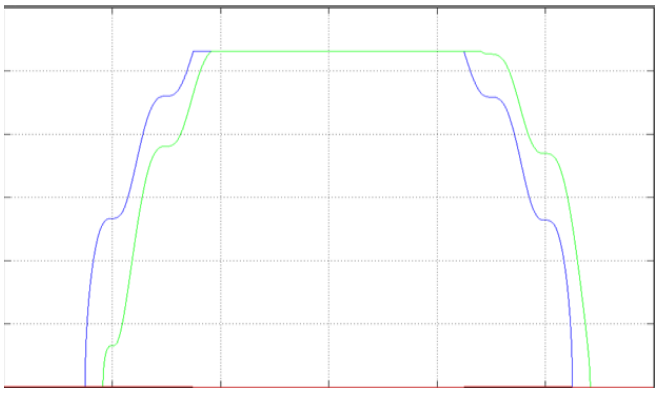

Fig. 3: Injected voltage magnitude for the depressed phases

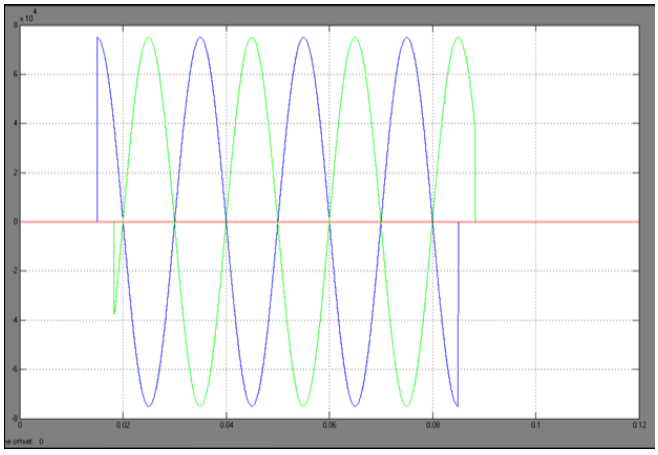

Fig. 4: Injected voltage for depressed phases

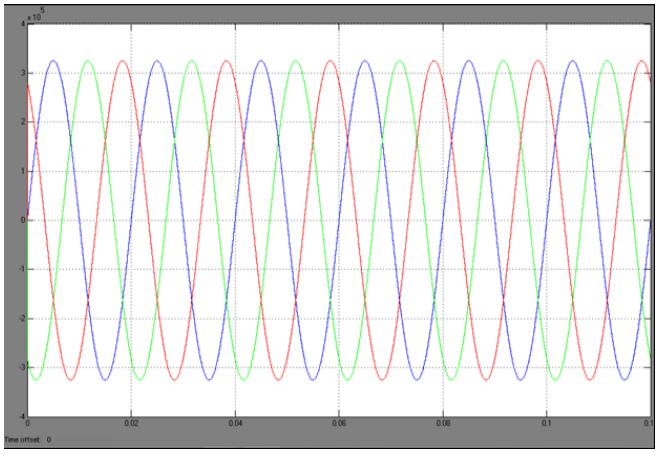

Fig. 5: Restored load voltage

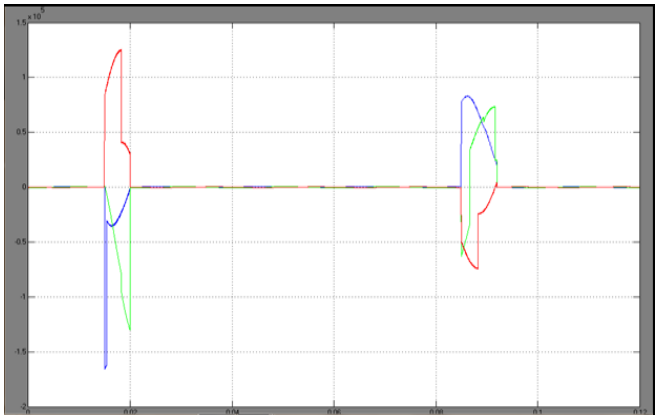

Fig. 6: Instantaneous load voltage error

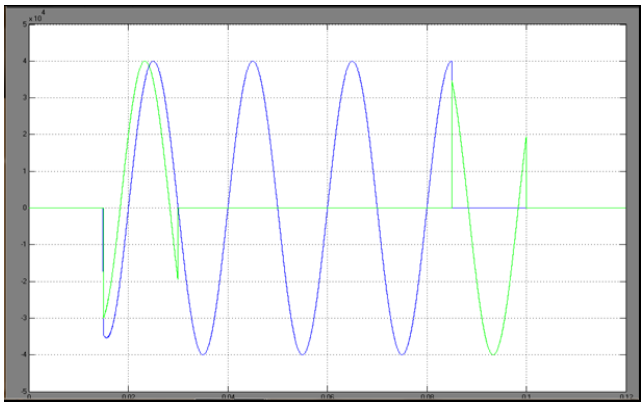

Fig. 7: Negative sequence components of the grid side voltages

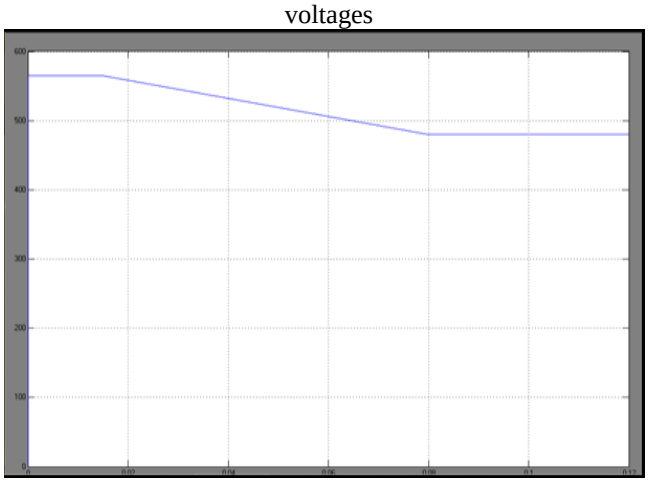

Fig. 8: DC link voltage

V. CONCLUSION

This paper proposes a novel control strategy for independent control of the injected voltages in each phase of the DVR to interrupt downstream fault currents in a radial distribution feeder. The proposed control strategy effectively compensates the load voltage zero- and negative-sequence components, as well as the positive-sequence component. This enables the DVR to restore the load voltages during balanced and unbalanced sags, in a short time interval (5 ms), with zero steady-state error. This control function is an addition to the voltage-sag compensation control of the DVR. The performance of the proposed controller can be observed using different fault scenarios, in which arcing fault conditions are included. The simulation studies demonstrate that the proposed multiloop control system comprises of an

outer control loop (voltage phasor control) and an inner control loop (instantaneous voltage control). The damping is provided by inner loop for which the transients are caused by the DVR harmonic filter. Hence, the dynamic response and stability of the DVR can be improved efficiently. The inner loop is shared by the sag compensation and the FCI functions. When a downstream fault is detected, the injected voltage magnitude and phase angle is controlled by outer loop of the faulty phase(s). Thus the load-side voltage is reduced to zero. This interrupts the fault current and the PCC voltage is restored. This proposed control system also performs satisfactorily under downstream arcing fault conditions.

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Ms. M. Prasanthi received the B.Tech Degree in Electrical & Electronics Engineering from Aditya Institute of Technology & Management, Tekkali, Srikakulam, India in 2012. Currently persuing M.Tech in Aditya Institute of Technology and Management, Tekkali Srikakulam, India. Her research interests include power quality and power electronics.

Dr. D.Vijaya Kumar completed his graduation in Electrical and Electronics Engineering from Andhra University, Visakhapatnam in 1997 and received his M.E.in Power Systems from Andhra University, India in 2000.He served as an Assistant Professor and Associate Professor in various Engineering colleges during 2000-2010 and at presently working in Department of Electrical and Electronics Engineering as a professor, AITAM College of Engineering, Tekkali, Srikakulam. His areas of interest are Power system and Control system.