

VLSI Implementation and Performance Evaluation of Low Pass Cascade & Linear Phase FIR Filter

Jaya Gupta, Arpan Shah, Ramesh Bharti

Abstract— In this paper, we present a VLSI implementation of low pass cascade & linear phase FIR filter for low power design. A dynamic power can be control using power supply. We proposed a VHDL implementation of low pass FIR filter. A output of the system in discrete form will transfer to MATLAB for frequency response generation. To make the pipelining more synchronous we have use a array based ROM to store inter-stage output. A cascade & linear phase FIR will be placed in the system and power consumption and frequency response will analysis.

Index Terms— FIR, Dynamic power, ROM

I. INTRODUCTION

A finite impulse response (FIR) filter is a filter whose impulse response is of finite duration or response to any finite length input, because it settles to zero in finite time [1]. The impulse response of an Nth-order discrete-time FIR filter lasts exactly N + 1 sample from first nonzero element through last nonzero element, before it then settles to zero. FIR filter can be discrete-time or continuous-time and digital or analog [2].

FIR filter output is shown by following equation,

$$y[n] = \sum_{k=0}^{N-1} h_k \cdot x[n-k] \quad (1)$$

$x[n]$ represents the filter input.

H_k represents the filter coefficients.

$y[n]$ represents the filter output.

N is the number of filter coefficients (order of the filter).

On taking z-transform of the above equation we get,

$$Y(z) = h_0X(z) + h_1z^{-1}X(z) + h_2z^{-2}X(z) + \dots + h_{N-1}z^{-(N-1)}X(z) \quad (2)$$

The equation of $Y(z)$ can be directly represented by a block diagram as shown in fig 1 and this structure is called Direct form structure or Fd.R filter [3]. The direct form structure provides a direct relation between time domain and z-domain equations.

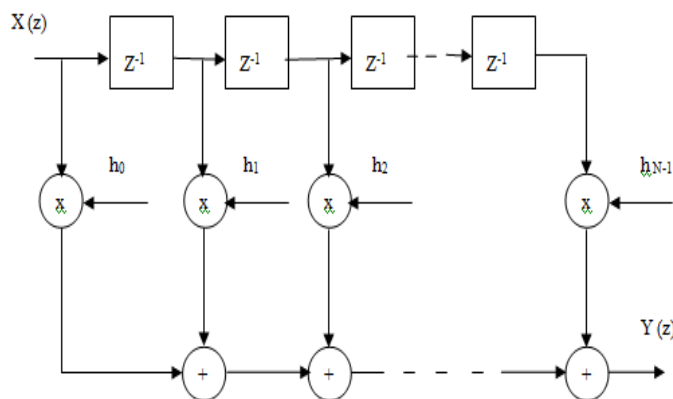


Fig 1 Direct Form structure of FIR Filter

The frequency response of FIR filter is presented by $H_d(e^{j\omega})$. So the equation for DFT coefficients $H(k)$ can be written as

$$H(k) = H_d(e^{j\omega}) \Big|_{\omega = \frac{2\pi k}{N}} = e^{-j\alpha\omega_k} \quad (3)$$

Where $\alpha = \frac{N-1}{2}$, $k=0, 1, \dots (N-1)$

The samples of impulse response $h(n)$ is given by,

When N is odd,

$$h(n) = \frac{1}{N} \left[H(0) + 2 \sum_{k=1}^{\frac{(N-1)}{2}} \text{Re} \left[H(k) e^{\frac{j2\pi nk}{N}} \right] \right] \quad (4)$$

When N is even,

$$h(n) = \frac{1}{N} \left[H(0) + 2 \sum_{k=1}^{\frac{(N-1)}{2}} \text{Re} \left[H(k) e^{\frac{j2\pi nk}{N}} \right] \right] \quad (5)$$

Now the Transfer Function $H(z)$ of the filter is given by z-transform of $h(n)$.

$$H(z) = \frac{Y(z)}{X(z)} = \sum_{n=0}^{N-1} h(n)z^{-n} \quad (6)$$

The magnitude response $|H(e^{j\omega})|$ is given by $A(\omega)$, where

$$A(\omega) = h\left(\frac{N-1}{2}\right) + \sum_{n=1}^{\frac{N-1}{2}} 2h\left(\frac{N-1}{2} - n\right) \cos(\omega n) \quad (7)$$

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Here $\omega = 0, \frac{\pi}{16}, \frac{\pi}{8}, \frac{3\pi}{16}, \dots, 2\pi$

The frequency response $H(e^{j\omega})$ is given by,

$$H(e^{j\omega}) = H(z) \Big|_{z=e^{j\omega}} \tag{8}$$

II. CASCADE AND LINEAR PHASE FIR FILTER

A. Cascade FIR Filter

The transfer function of a FIR system,

$$H(z) = \frac{Y(z)}{X(z)} = h_0 + h_1z^{-1} + h_2z^{-2} + \dots + h_{N-1}z^{-(N-1)} \tag{9}$$

The transfer function of FIR system is (N-1)th order polynomial in z. As a alternative to the Direct form [4], this polynomial can be factorized into first and second order factors and the transfer function H (z) can be expressed as a product of first and second order factors or sections as shown in equation [5],

$$H(z) = \frac{Y(z)}{X(z)} = H_1(z) \times H_2(z) \times H_3(z) \dots H_N(z) = \prod_{i=1}^N H_i(z) \tag{10}$$

Where,

$$H_i(z) = h_{0i} + h_{1i}z^{-1} + h_{2i}z^{-2} \quad ; \text{ Second order section}$$

Or,

$$H_i(z) = h_{0i} + h_{1i}z^{-1} \quad ; \text{ First order section}$$

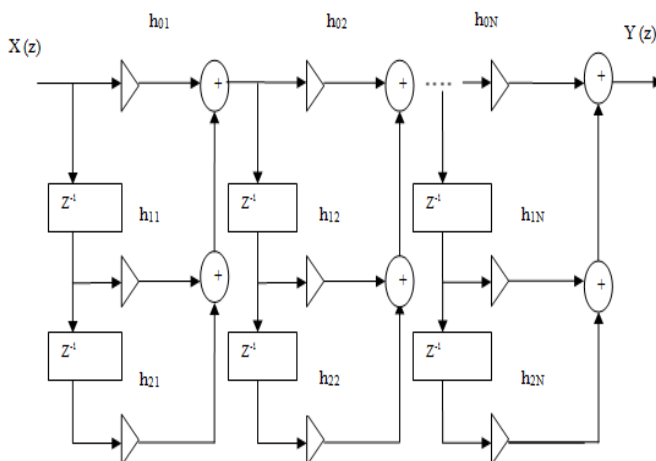
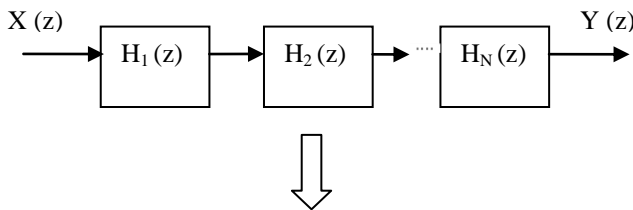


Fig 2 Cascade structure of FIR Filter

The individual second order or first order sections can be realized either in direct form structure or linear phase structure [6]. The overall system is obtained by cascading the individual sections as shown in fig 2. The number of calculations and the memory requirement depends on the realization of individual sections [7].

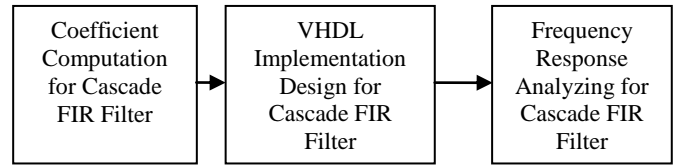


Fig 3 Block Diagram of Implementation of Cascade FIR Filter

Algorithm:

1. We calculate the coefficients with the help of following formula using MATLAB.

$$h(n) = \frac{1}{N} \left[H(0) + 2 \sum_{k=1}^{\left(\frac{N-1}{2}\right)} \text{Re} \left[H(k) e^{\frac{j2\pi nk}{N}} \right] \right]$$

2. In VHDL implementation, find the output of first stage as $H_1(z)$.
 - a) Multiply the input with coefficient.
 $M_n = X(z) * h_n$
 - b) Now add all the multiplicants to find the output of first stage.
3. Similarly in next two stages of cascade structure we repeat the 2nd step.
4. Thus we calculate the output of last stage as final output Y (z).
5. Now frequency response generated by using MATLAB.

B. Linear phase FIR Filter

If the impulse response is symmetric about its origin, linear phase results. If all zero filter has a linear phase response, a special non-recursive structure that reduces the number of multiplications by approximately one half can be implemented. The impulse response for a casual filter begins at zero and ends at N-1 [8].

A linear phase FIR filter of length N is characterized by

$$h(n) = h(N - 1 - n) \tag{11}$$

The symmetry property of a linear phase FIR filter is used to reduce the multipliers required in these realization [9]. Using this condition, the z-transform of the impulse response can be expressed as

$$H(z) = Z[h(n)] = \sum_{n=0}^{N-1} h(n)z^{-n} \tag{12}$$

For N even,

$$H(z) = \sum_{n=0}^{\frac{N}{2}-1} h(n) [z^{-n} + z^{-(N-1-n)}] \tag{13}$$

The output transform

$$Y(z) = H(z)X(z) = h(0)[1 + z^{-(N-1)}]X(z) + h(1)[z^{-1} + z^{-(N-2)}]X(z) + \dots + h\left(\frac{N}{2}-1\right)\left[z^{-\left(\frac{N}{2}-1\right)} + z^{-\frac{N}{2}}\right]X(z) \tag{14}$$

Here $N/2$ multipliers are required [10].

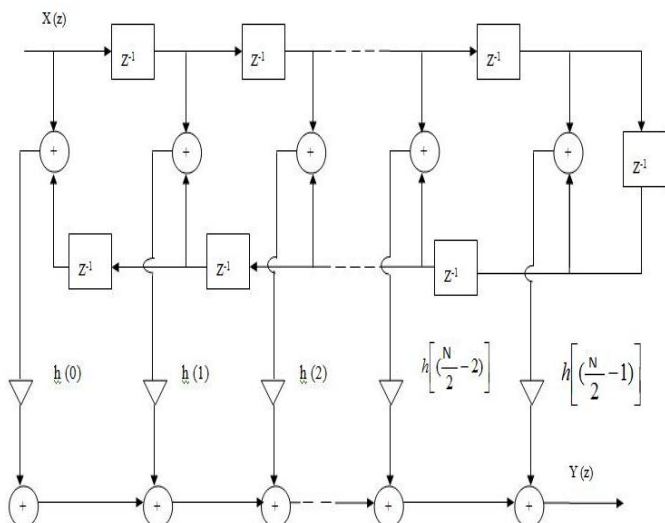


Fig 4 Linear phase structure of FIR Filter when N is even

For N odd,

$$H(z) = h\left(\frac{N-1}{2}\right)z^{-\frac{(N-1)}{2}} + \sum_{n=0}^{\frac{N-3}{2}} h(n) \left[z^{-n} + z^{-(N-1-n)} \right] \quad (15)$$

Here $\left(\frac{N+1}{2}\right)$ multipliers are required [11].

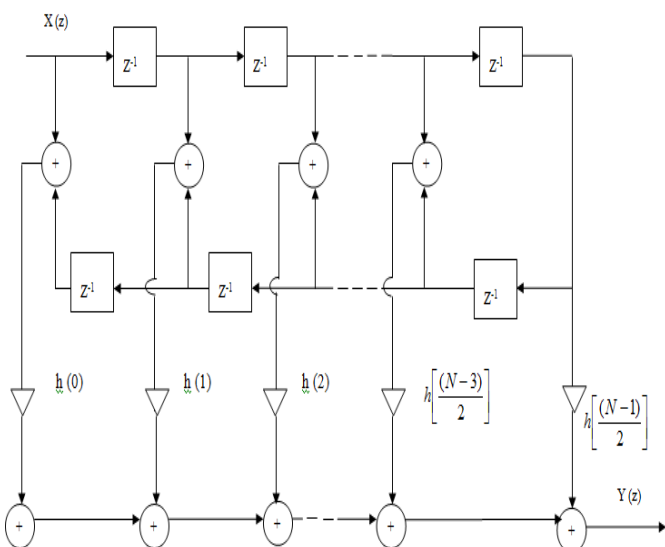


Fig 5 Linear phase structure of FIR Filter when N is odd

The linear phase FIR system recognition require approximately only half the number of multipliers than direct form and cascade form realizations [12]. The samples obtained by sampling ideal frequency response are DFT coefficients. The complex DFT coefficients obtain by sampling frequency response always exist as conjugate pairs [13].

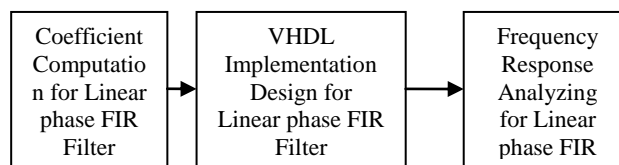


Fig 6 Block Diagram of Implementation of Linear Phase FIR Filter

Algorithm:

1. We calculate the coefficients with the help of following formula using MATLAB.

$$h(n) = \frac{1}{N} \left[H(0) + 2 \sum_{k=1}^{\frac{(N-1)}{2}} \text{Re} \left[H(k) e^{\frac{j2\pi nk}{N}} \right] \right]$$
2. In VHDL implementation, find the output $Y(z)$ of proposed design of linear phase FIR filter .
 - a) We separate the inputs into 1st stage and 2nd stage.
 - b) Now add the first input of first stage with last input of second stage and then increase the input of first stage and decrease the input of second stage. $L = Q_1 + Q_{10}$
 - c) Now multiply the result of above addition with coefficients.
 - d) Now add all the multiplicands to find the output.
3. Now frequency response generated by using MATLAB.

III. RESULT

Area(no. of LUT)

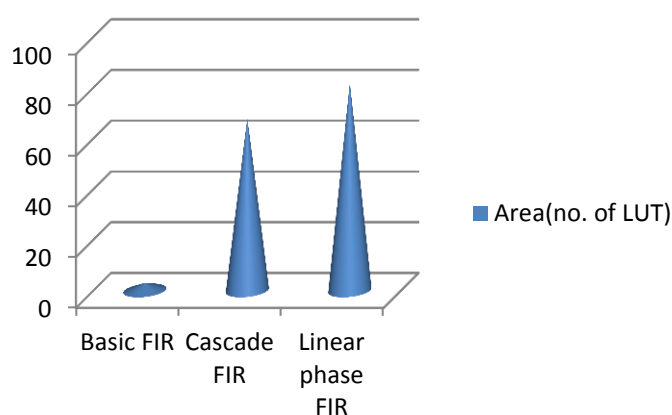


Fig 7 Graphical Comparison of Area

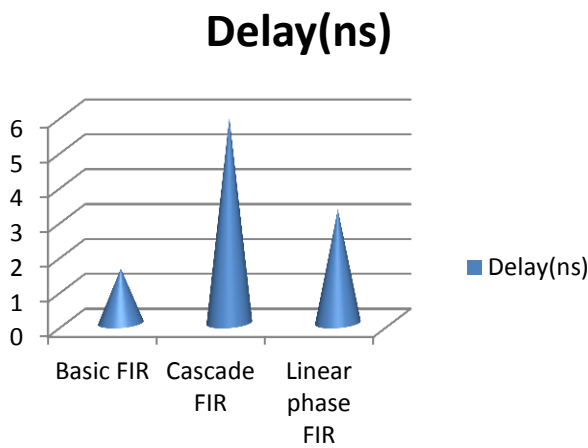


Fig 8 Graphical Comparison of Delay

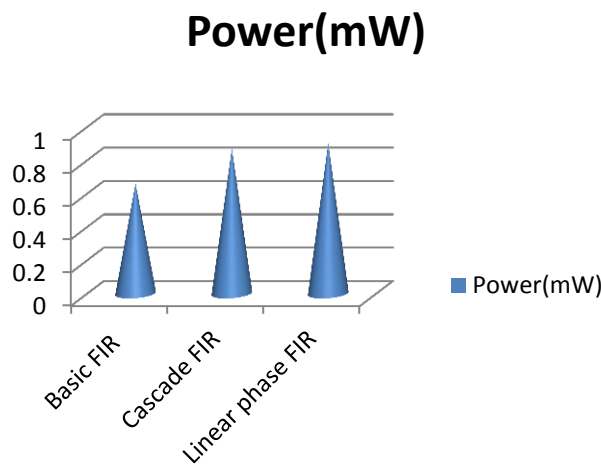


Fig 9 Graphical Comparison of Power

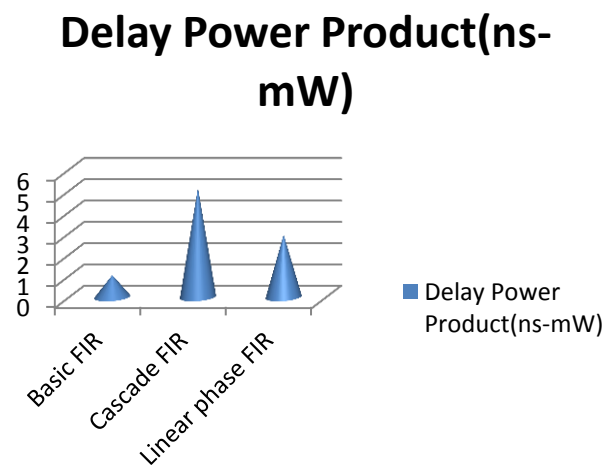


Fig 10 Graphical Comparison of Delay*Power

Name of filter	Area (no. of LUT)	Speed delay(ns)	Power (mW)	Delay power product (ns-mW)
Basic FIR	3	1.558	0.662	1.031
Cascade FIR	68	5.898	0.872	5.143
Linear phase FIR	82	3.259	0.903	2.942

Table 1 Overall Comparison of Basic FIR, Cascade FIR and Linear Phase FIR Filters Design

IV. CONCLUSION

Table 1 shows the Overall Comparison of Basic FIR, Cascade FIR and Linear Phase FIR Filters Design. It is clear that there is a decrease in circuitry, power consumption of Cascade FIR as compared to the Linear Phase FIR design But an increase in time consumption of Cascade FIR as compared to the Linear Phase FIR design. The overall product of delay (ns) and power (mW) of Linear Phase Filter is reduced by 42.79% as compared to Cascade Filter, which shows the improvement in Linear Phase FIR Filter Design results.

REFERENCES

- [1] "A low-power digit-based reconfigurable FIR filter", K.-H. Chen and T.-D. Chiu, IEEE Transaction Circuits Syst. II, vol. 53, no. 8, pp. 617–621, August 2006.
- [2] "The multiplexed structure of multi-channel FIR filter and its resources evaluation", L. Ming and Y. Chao, in Proc. Int. Conference. CDCIEM, pp. 764–768, Mar. 2012.
- [3] "Reconfigurable architecture of a RRC FIR interpolator for multi-standard digital up converter", Hatai, I. Chakrabarti, and S. Banerjee, in Proc. IEEE 27th IPDPSW, pp. 247–251, May 2013.
- [4] "FPGA realization of FIR filters by efficient and flexible systolization using distributed arithmetic", P. K. Meher, S. Chandrasekaran, and A. Amira, IEEE Trans. Signal Process., vol. 56, no. 7, pp. 3009–3017, July. 2008.
- [5] "Dynamically reconfigurable FIR filter architectures with fast reconfiguration", M. Kumm, Moller, and P. Zipf, in Proc. 8th Int. Workshop ReCoSoC, pp. 1–8, Jul. 2013.
- [6] "High-throughput pipelined realization of adaptive FIR filter based on distributed arithmetic", P. K. Meher and S. Y. Park, in Proc. IEEE/IFIP 19th Int. Conf. VLSI-SOC, pp. 428–433, Oct. 2011.
- [7] "Adaptive filters using modified sliding-block distributed arithmetic with offset binary coding", W. Huang and D. V. Anderson, in Proc. IEEE In. Conf. Acoust., Speech, Signal Process. (ICASSP), pp. 545–548, 2009.
- [8] "Delayed block LMS algorithm and concurrent architecture for high-speed implementation of adaptive FIR filters", B. K. Mohanty and K. Meher, presented at the IEEE Region 10 TENCON 2008 Conf., Hyderabad, India, Nov. 2008.
- [9] "Two high-performance adaptive filter implementation schemes using distributed arithmetic", R. Guo and L. S. DeBrunner, IEEE Trans. Circuits Syst. II, vol. 58, no. 9, pp. 600–604, September 2011.
- [10] "FPGA implementation of fast block LMS adaptive filter using distributed arithmetic for high-throughput", S. Baghel and R. Shaik, in Proc. Int. Conference. Commun. Signal Process. (ICCSPP), pp. 443–447, Feb. 10–12, 2011.
- [11] "Low power and less complex implementation of fast block LMS adaptive filter using distributed arithmetic", Baghel and R. Shaik, in Proc. IEEE Students Technol. Symp., pp. 214–219, January 14–16, 2011.

- [12] "Design and realization of FIR digital filters based on MATLAB" Chonghua Li, IEEE Anti-Counterfeiting Security and Identification in Communication (ASID), 2010 International Conference, ISBN no. 978-1-4244-6731-0, pp. 101 – 104, 18-20 July 2010.
- [13] "Design of Digit-Serial FIR Filters: Algorithms, Architectures, and a CAD Tool", Aksoy L., Lazzari C., Costa E., Flores P and Monteiro J, IEEE Transactions, Vol. 21, Issue 3, pp. 498 – 511, ISSN no. 1063-8210, March 2013.
- [14] "Linear phase low pass FIR filter design using Improved Particle Swarm Optimization", Mukherjee S., Kar R., Mandal D. and Mondal S., Research and Development (SCORED), 2011 IEEE Student Conference, ISBN no. 978-1-4673-0099-5, pp. 358 – 363, 19-20 Dec. 2011.

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