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Analysis of Different CMOS Full Adder Circuits Based on Various Parameters for Low Voltage VLSI Design

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Abstract— **The demand for portable consumer electronics products is increasing at extremely high rate in recent years; therefore development of low-power VLSI circuits is essential. To achieve this objective a lot of innovative work has been done in this field, many innovative designs for basic logic functions have appeared. Various adders are used for implementing these logic functions which are most important components in digital design. The performance of these full adders can be measured in terms of propagation delay, power dissipation and power delay product.**

In this paper the performance of eleven different 1-bit full adder cells based on different logic styles are evaluated. The framework includes evaluation performance of different logic styles including an input test pattern which are analyzed with respect to power, delay and power-delay product.

Evaluating the performance of a full adder cell is categorized on the basis of three different types of analysis:

1. **Comparison of full adders on the basis of power, delay and power-delay product at 1V.**
2. **Comparison of full adders on the basis of power, delay and power-delay product based on different input patterns.**
3. **Comparison of full adders on the basis of power, delay and power-delay product based on different supply voltage.**

Cadence VIRTUOSO environment is used for making schematics on 45 nm technology and SPECTRE is used for running simulations. The supply voltage used in the simulation work is 1 V.

All three analyses shows that 10-Transistor full adder features good delay performance, demonstrates better delay product and consumes lower power as compared to entire eleven full adder because it is a Hybrid logic style. 10T is low power implementation and it has lower loading of the inputs and intermediate nodes, lower transistor count and a balanced generation of Sum and C_{out} signal. These are the reason why 10-Transistor full adder circuit performances exceptionally good at lower technologies.

Index Terms— **Complementary Metal Oxide Silicon (CMOS),Conventional CMOS Full Adder, Low Voltage VLSI Design,Gate diffusion full adder,Transistor Full Adder**

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I. INTRODUCTION

Electronics dominates the world today and many of the people in it. The semiconductor industry has witnessed an explosive growth of integration of sophisticated multimedia-based applications into mobile electronics gadgetry since the last decade. The development of low power circuits faces tremendous challenges as service increases. This leads to remarkable growth in research that particularly aims on development of low power synthesis tool. Addition is one of the most vital and elementary operation that describe whole performance of the system. It is used extensively in many VLSI systems such as microprocessors and application specific DSP architecture. Evolution in the field of mobile communication and computers has attracted the focus of researchers on smaller silicon area, higher speeds, longer battery life and more reliability. As the CMOS process technology shrinks, it has driven the VLSI industry towards very high integration density and system on chip designs and beyond few GHz operating frequencies, critical concerns have been arising to the severe increase in power consumption and the need to further reduce it.

The main task of a full adder is to add two or more binary numbers and it serves the nucleus of many other useful operations. Adder lies in the critical path of most of the applications, therefore it determines the overall system performance. Building block of binary adders is a 1-bit adder. As a result of which, the performance of entire system is enhanced on enhancing performance of a 1-bit adder.

Digital circuit designers have been encountered in a trade-off between speed and power consumption to improve their design's performance. Different logic styles tend to favour one performance aspect at the expense of the others. The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit. Low power circuit design has been a challenge for a long time. Low power can be achieved at four different levels of the design process, the circuit, the architectural, the device or the layout levels. Fast arithmetic computation cells including adders and multipliers are the most frequently and widely used circuits in VLSI systems. The adders are basic building blocks in various circuits' especially arithmetic circuits, compressors, comparators, parity checkers, code converters, error-detecting or error-correcting codes and phase detector. Although all adders have similar function, the way of producing the intermediate nodes and the transistors count is varied.

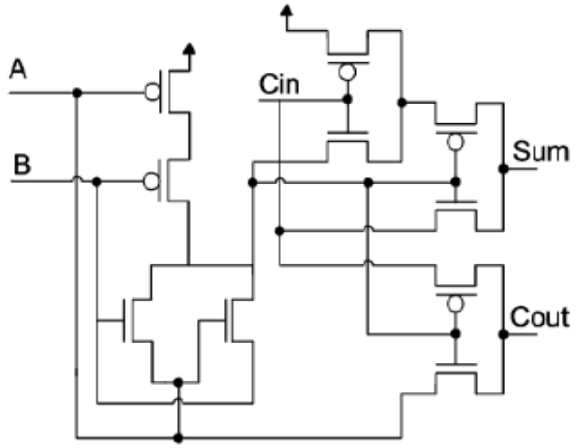

Figure- 10-Transistor Adder

II. LITERATURE SURVEY

In recent years, several types of different logic styles have been proposed to implement 1-bit adder cells. Full adder circuits are classified into two groups on the basis of output. The first groups of full adders have full swing output. C-CMOS, CPL, TGA, TFA, Hybrid, 14T and 16T belong to the first group .

First group have good driving ability, high number of transistors, large areas and usually higher power consumption in comparison to the second group.

Second groups comprises of full adders (10T, 9T and 8T) without swing outputs. These full adders usually have low number of transistors (3T) based XOR-XNOR circuits, less power consumption, and less area occupation. The non full swing full adders are useful in building up larger circuits. One such application is the Manchester Carry Look Ahead chain.

Vahid Foroutan, Keivan Navi and Majid Haghparast presented a new low power dynamic CMOS 1-bit full adder cell by eliminating the time consuming XOR gates from the design. They also tell that with the lowering of threshold voltage in ultra deep submicron technology, lowering the supply voltage appears to be the most eminent means to reduce power consumption. However, lowering supply voltage also increases circuit delay and degrades the drivability of cells designed with certain logic styles. Most of these adders lack driving capabilities in fan-out situation and the performance of these circuits degrade drastically when they are cascaded. The main drawback of static logic style is the lack of performance, but in dynamic CMOS logic style which provides a high speed of operation this drawback is eliminated.

Reza Faghih Mirzaee, Mohammad Hossein Moaiyeri, Keivan Navi presented two novel 1-bit full adder cells in dynamic logic style. NP-CMOS (Zipper) and Multi-Output structures are used to design the adder blocks. According to them characteristic of dynamic logic leads to higher speeds than the other standard static full adder cells. The authors have used HSpice and 180 nm CMOS technology, which exhibits a significant decrease in the cell delay which can result in a considerable reduction in the power-delay product (PDP). They have calculated the PDP of Multi-Output design at 1.8v power supply which comes around 0.15 femto-joules that is 5% lower than conventional dynamic full adder cell and at least 21% lower than other static full adders.

On the basis of Logic style full adders are divided into three categories:-

Static: More reliable**,** simpler, lower power consuming

Dynamic: Fast switching speed, no static power consumption, non ratio logic, full swing voltage, lesser number of transistors, less area. This makes reduction in the capacitive load at the output node.

Hybrid: Both dynamic and static.

Dynamic required an N input logic function requires N+2 transistors versus 2N transistors in the standard CMOS logic. The area advantage comes from the fact that the PMOS network of a dynamic CMOS gate consists of only one transistor. This also results in a reduction in the capacitive load at the output node, which is the basis for the delay advantage. There are various issues related to the full adder like power consumption, performance, area, noise immunity , regularity and good driving ability. Many researchers have combined these two structures and have combined these two structures and have proposed hybrid dynamic static full adders.

III. RESEARCH ELABORATION

IMPLEMENTATION OF ADDERS

1. 10-Transistor Full Adder

10 Transistor full adder use more than one logic style for the implementation and it is known as Hybrid logic design style. The number of transistors count is 10, as shown in figure. A, B and C_{in} are the inputs and Sum & C_{out} are the outputs. 10T generates A XOR B and use it along with its complement as a select signal to generate the output. The full adder is made to work on 1 volt since 45nm technology is used. In full adder 10T small number of transistor count are used and produces the non full swing pass transistor with the full swing restored transmission gate technique. 10T has the smaller delay because of its supply voltage. It produces high capacitance values for the inputs; this is the only disadvantage in full adder 10T. 10T have lower loading of the inputs and intermediate nodes, lower-transistor count and balanced generation of Sum and C_{out} signal. When 10T and 14T are cascaded, full adder lack driving capability in fan out situation and even its performance degrades. Full adder using 10T is simulated in CADENCE VIRTUOSO with 45nm in 1 V.

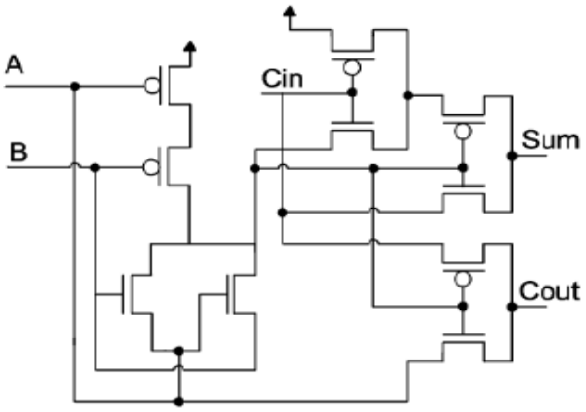

Figure - 10-Transistor Adder

2. Complementary Pass Transistors Full Adder

The CPL(Complementary Pass Transistors) Full Adder has 18 transistors and is based on NMOS pass-transistor logic. This causes low input capacitance and high speed operation. However it also leads to threshold voltage loss in the output circuit. CPL consumes less power than standard static CMOS circuits, due to less output swing. However it reduces noise margin and causes serious problems in cascading, especially in low voltages. Therefore, CMOS inverters are used to restore the outputs voltage level and ensure the drivability, and feeble PMOS transistors are used to minimize the static current caused by the incomplete turn-off of the PMOS in the output inverter. The advantages of the CPL style are the small input capacitance, low internal voltage swing, good output driving capability due to the output inverters, and a fast differential stage.

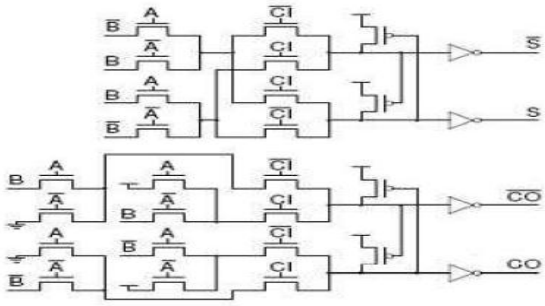

Figure - CPL Adder

3. Transmission Gate Full Adder

Transmission Gate Full Adder (TGA) is one of the full adder implementation techniques. TGA circuit is based on transmission gate. Transmission gate full adder consists of 20 transistors. TFA consists of a PMOS transistor and NMOS transistor that are connected in parallel way, which in particular type of pass transistor logic circuits. A, B and C_{in} are the inputs and Sum and C_{out} are the outputs. There is no voltage drop problem but it requires double the number of transistors to design the function. It consumes low power therefore it is good for designing XOR or XNOR gates.

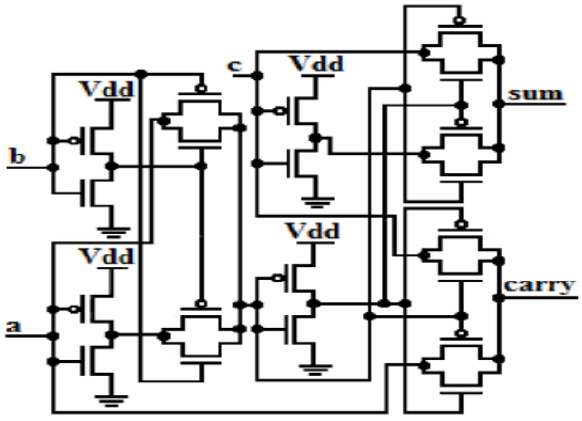

Figure - Transmission Gate Full Adder

4. Conventional CMOS Full Adder

Conventional CMOS Full Adder is the most basic full adder implementation techniques. Conventional CMOS Full Adder consists of 28 transistors. A, B and C_{in} are the inputs and Sum & C_{out} are the outputs. Static logic provides robustness against noise effects, so automatically provides a reliable operation. Pseudo NMOS pass-transistor logic and reduce the number of transistors required to implement a given logic function but these suffer from static power dissipation. On the other hand, dynamic logic requires less silicon area for implementation of complex function but charge leakage and charge refreshing are required which reduces the frequency of operation. This circuit uses both NMOS and PMOS transistors. In Conventional CMOS Full Adder, there are many leakage paths which lead to more sub threshold leakage.

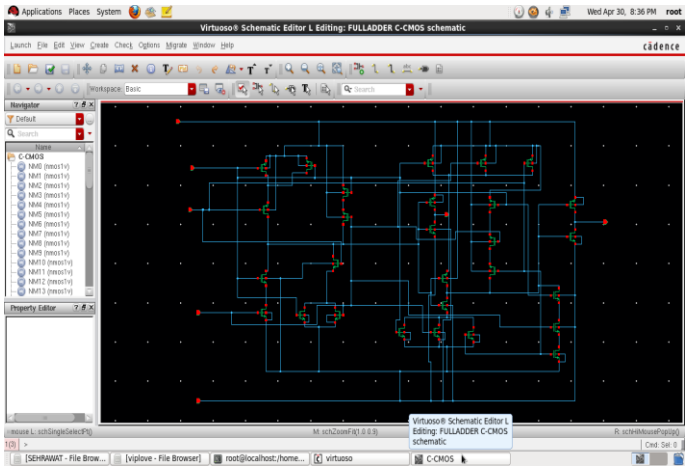

Figure - Schematic of C-CMOS Adder

5. P-XOR and G-XOR Based Full Adder

It resembles the inverter-based XOR but the difference is that the VDD connection in the inverter-based XOR is connected to the input A. Since the new XOR gate has no power supply, it is called Powerless XOR, or P-XOR. A new XNOR gate is named as Groundless XNOR or G-XNOR because there is no direct connection with ground. 9B and 13A are the adders which are implemented using this technique. The addition of 2 bits A and B with C_{in} yields a Sum and C_{out} bit. These adders are having low power consumption and better speed performances.

In power consumption, adder 9B consistently has better power consumption than the SERF adder. The CMOS adder dissipates more power than the other adders. Adders 13A and 9B have better speed than the SERF adder. The basic disadvantages of these full adders are that it suffers from the threshold-voltage loss of the pass transistors. They all have double threshold losses in full adder output terminals. This problem usually restricts the full adder design from operating in low voltage or cascading without extra buffering. The lowest possible power supply is limited to $2V_{tn}+V_{tp}$ where V_{tn} and V_{tp} are the threshold voltages of NMOS and PMOS respectively.

6. Gate Diffusion Input Full Adder

Full adder cell with the GDI technique is implemented to design a high performance and low power full adder. GDI cell contains three inputs- G (common state input of NMOS and PMOS), N (input to the source or drain of NMOS) and P (input to the source or drain of PMOS). A, B, C_{in} are taken as one bit input for one bit full adder and generated outputs are SUM and CARRY. Full adder cell comprises of 10 transistors. Full adder is divided into two stages; GDI technique is used in first cell to generate XOR and XNOR functions. Full swing with low voltages is shown in first stage

and complementary outputs with other inputs will be fed to the second stage in which Sum and Carry are generated. Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter. The only state where low swing occurs in the input value is A=0, B=0. In this case, the voltage level of F1 is V_{tp} (instead of the expected 0 V) because of the poor high to low transition characteristics of the PMOS pass transistor. The effect occurs only in the transition from A=0, B=V_{dd} to A=0, B=0. In some cases, when V_{dd}=1 without a swing drop from the previous stages, a GDI cell functions as an inverter buffer and recovers the voltage swing, although this feature allows a self-swing restoration in certain cases.

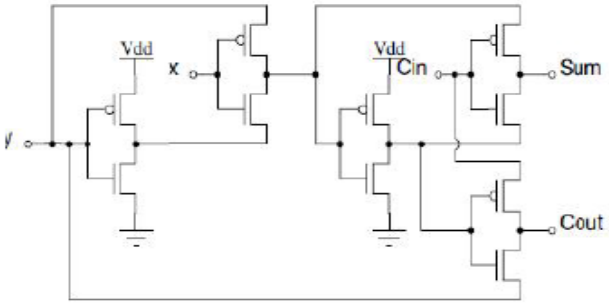

Figure - Gate Diffusion Input Full Adder

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IV. RESULT AND DISCUSSION

1. Simulation Environment

Cadence VIRTUOSO environment have been used for evaluating time delay and power dissipation using 45 nm CMOS technology at room temperatures for comparing 1-bit full adder performances. Simulation has been performed for different supply voltages ranging from 0.6 to 1.4 V.

The main advantage of using this simulation environment is that the power components are taken into account, in addition to the dynamic one.

1. Five input patterns with different transition are applied to entire 11 full adders to calculate power, delay and PDP. Furthermore, the energy required to charge and discharges the DUT (device under test) internal nodes when the module has no direct power supply connection, comes through the DUT inputs.

2. Test input patterns as the input combination necessary to determine the worst case propagation delay and power dissipated values.

3. The short-circuit consumption of the DUT by itself, as it is receiving signal with finite slopes coming from the input, instead of ideal ones coming from voltage sources.

4. Common input pattern is voltage scaled and is applied to all eleven adders to calculate power dissipation and propagation delay.

2. Comparison of Full Adders on the Basis of Power, Delay and PDP

The circuit simulator used to obtain the various parameters for comparison is 'SPECTRE' on VIRTUOSO Cadence layout suite. Technology being used is 45 nm.

To perform a comparative study of performances of various full adder circuits, we need to apply the same input pattern to all of them. The input test pattern we have used consists of three input signals, A, B and C_{in}, and these signals are square waves of equal on and off times.

Before transistor resizing the output waveform obtained is not perfectly sharp and glitches occur. Among the three inputs of a full adder (A, B, C_{in}), inputs A and B are assumed to be perfect and might not be degraded due to the threshold voltage loss since V_{IH} and V_{IL} for inputs A and B are V_{DD} and ground respectively. However input Carry is drawn from the output Carry of another full adder so it might be degraded due to threshold voltage loss.

After transistor resizing i.e adjusting W/L ratio, the irregularities and glitches are reduced to an acceptable level in the output waveform as shown figure.

There is a minute increment in power dissipation after applying transistor resizing, but overall effect on the performance of transistor is very good, therefore we apply transistor resizing to all the 1-bit full adders. This results in better performance and improved efficiency by reducing delay and power delay product.

$$\left(\frac{W1}{L1}\right)\mu_n = \left(\frac{W2}{L2}\right)\mu_p \qquad (1)$$

Where W is the width of NMOS and PMOS, L is length of channel, μ_n and μ_p are mobility of electrons and holes respectively.

So, By the calculations results are as follow-

S. No.	Adder Cell	No. of Transistors	Technology	Supply Voltage	Power (nW)	Delay (ps)	PDP (aJ)
1	CMOS	28	45 nm	1 V	18400	110.8	2038
2	CPL	38	45 nm	1V	272.9	59.11	16.07
3	TFA	16	45 nm	1V	$2.3*10^6$	48.01	114240
4	TGA	20	45 nm	1V	200.8	55.51	11.146
5	9B	10	45 nm	1V	111.7	86.62	9.675
6	13A	10	45 nm	1V	189.8	10.69	2028.9
7	GDI	10	45 nm	1V	130.2	83.1	10.81

Where,

CPL Complementary Pass Transistor Full Adder

TFA 14-Transistor Full Adder

TGA Transmission Gate Full Adder

9B P-XOR Based Full Adder

13A G-XOR Based Full Adder

GDI Gate Diffusion Input Full Adder

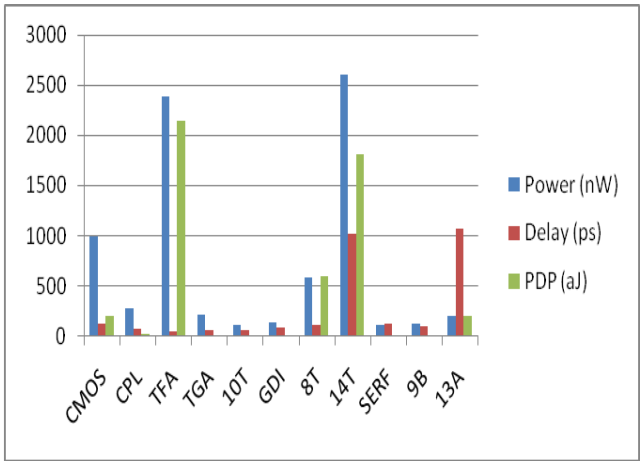

Figure- Comparison of all Full Adders with their Power (nW), delay (ps) and PDP (aJ).

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