Simulation and Design Analysis of Integrated Receiver System for Millimeter Wave Applications

Suraj Pratap, Rajesh Parihar

Abstract— **T***he objective of this research was to define a methodology for designing* **presents the simulation and design analysis of fully integrated receiver system for millimeter and microwave applications. A beauty thought of new design of CMOS LNA, filter and micro strip antenna are largely improves the system integration, reduced chip area and save the cost. In this paper, a three different architecture are proposed and analyzed through Agilent ADS tool. We have designed 90nm CMOS LNA at 40GHz to integrate with band pass filter and rectangular patch antenna at same frequency.**

Index Terms—**CMOS LAN, ADS TOOL.**

I. INTRODUCTION

Today, fastest growth of wireless communication industries is establishing a big new market opportunity. Current researchers are founding for new solutions which would be implemented into the existing wireless system networks to provide the broader bandwidth, the high quality and new added services. A millimeter wave (MMW) frequency band is the most promising technology for providing broadband wireless communications [1]. The extensive progress of CMOS technology has enabled its application in microwave and millimeter wave technologies. Presently, the CMOS technology has became one of the most attractive choices in implementing transceiver due to its low cost and high level of integration [2]. In spite of the advantages of CMOS technology, the design of CMOS transceiver in millimeter wave applications exhibits several challenges and difficulties that the designers must overcome. In addition, Kinetic performances of active devices with patch antenna have been improved, where MMW designs can be considered [7].

In RF receiver, the input signal from antenna first passes through the band pass filter to the LNA that amplifies it's and suppresses noise contributions from preceding stages. Hence, low noise figure and good impedance matching are essential . LNA performance parameters while high gain are required by receiver system for achieve the system reliability. In present scenario, a 40GHz three stage of CG-CS LNA are designed using 90nm CMOS technology and integrated to Co-design of patch antenna with filter to achieve more than 20dB gain with good reverse isolation parameter that is enough to prove the system reliability. The basic geometry of complete receiver system are shown in Fig.1

Suraj Pratap, CBS Group Institution Haryana

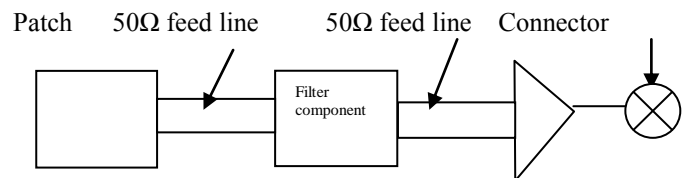**Rajesh Parihar,** Asst. Professor, CBS Group Institution Haryana

Fig.1 Basic geometry of LNA, filter and patch antenna

II. CMOS LNA ANALYSIS

As the fulfill requirements of LNA design, we can use the different topology like common source (CS), Common Gate (CG) etc. which are briefly discuss below.

A. CG-CS Topology

The common source (CS) and common gate (CG) LNA typologies are two popular architecture choices which are widely used for LNA design. The CS with the source inductor degeneration technique achieves the input impedance matching with the ideal noiseless components and gives to a minimal noise figure and also provides a higher gain whereas common gate has offers Wideband operating performance with good linearity and input-output isolation property [6]. But the parasitic capacitance of the transistor degrades the CGLNA performance in the higher frequency. The first stage of CGLNA is connected with the same next stage through a bonding wire can solve this problem and achieve the broadband operating performance which also holds the same beauties of the original CG LNA architecture at the same time [5]. Hence, we have design one stage CGLNA to achieve good reverse isolation with 50Ω proper impedance matching and single stage of CSLNA is added to the one stage CGLNA through a bonding wire which provides low noise and high gai

B. Circuit Design

A 40GHz two stage of CMOS LNA is designed using 90nm commercial TSMC design kit in Agilent advanced design system. Before proceed to LNA design, firstly we have analyzed the one stages of CGLNA with low Q factor and achieves the good reverse isolation (S_{11}) is -28dB and 50Ω input impedance with the help of equation given below and its simulation results are shown in Fig.3 and Fig.4 but sacrifice its noise figure and gain parameters.

$$Zin = \frac{1}{g_m + jwC_{gs}} \qquad (1)$$

$$S_{11} = 20.\log_{10}\left(\left|\frac{Z_{in} - R_S}{Z_{in} + R_S}\right|\right) \qquad (2)$$

For achieving the losses parameters (like noise figure, gain etc), we are using the next stage i.e. CS with source degeneration and achieved best gain of 26dB and minimum noise figure of 3.8dB which are shown in Fig.5 and Fig.6 as per specification of our design. Fig.2 shows the circuit schematic of the CMOS LNA at 40GHz. The cascode topology is used to reduce the miller effect, improve the stability and provides the higher power gain. The input-output match is accomplished with an LC impedance transformation network. The 208-fF output capacitor was implemented with two 218-fF capacitors in series to desensitize the process variation. Parasitic capacitances of input and output RF bond pads are also considered in the circuit simulation. In this simulation, we have chosen design specifications and technologies under low supply voltage of 1.8V are shown in Table1.

III. CONCLUSION

The complete receiver system is designed for MMW applications in this paper, based on CMOS technology. The double-ended three stages of LNA are designed using 90nm CMOS process at 40GHz in this circuit. Performance standards are met for this new design technique

REFERENCES

[1] *Analysis and Design*, 2nd ed. Upper Saddle River, NJ: Prentice G. Gonzalez, *Microwave Transistor Amplifiers* -Hall, 1997.

[2] Alireza Zolfaghari*, Member, IEEE,* and Behzad Razavi*, Fellow, IEEE,* "A Low-Power 2.4-GHz Transmitter/Receiver CMOS IC "Ieee Journal Of Solid-State Circuits, Vol. 38, pp.177-181, February 2003.

[3] A. Bevilacqua, and A.M.Niknejad, "An Ultrawideband CMOS low noise amplifier for 3.1-10.6GHz wireless receivers", IEEE Journal of Solid State Circuits, Vol. 39, No. 12, pp. 2259-2268, Dec. 2004.

[4] A. Ismail, and A.A.Abidi, "A 3-10GHz low-noise amplifier with wideband LC-ladder matching network," IEEE Journal of Solid State Circuits, Vol. 39, No. 12, pp. 2269-2277, Dec. 2004.

[5] D.J.Allstot, X.Li and S.Shekhar,"Design considerations for CMOS Low-Noise Ampliifers", in Proc. IEEE Radio Frequency Integrated Circuits(RFIC) Symp., pp. 97-100, June. 2004.

[6] H.Darabi, and A.A.Abidi,"A 4.5mW 900-MHz CMOS receiver for wireless paging", IEEE Journal of Solid State Circuits, Vol. 35, No. 8, pp. 1085-1096, Aug. 2000.

[7] Sébastien Montusclat, Fréderic Gianesello, Daniel Gloria, "Silicon full integrated LNA, Filter and Antenna system beyond 40 GHz for MMW wireless communication links" in advanced CMOS technologies. *IEEE SOICONF*, 2005.

[8] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, May 1997.

[9] Kuo-Jung Sun, Zuo-Min Tsai*, Student Member, IEEE*, Kun-You Lin*, Member, IEEE*, and Huei Wang*, Fellow, IEEE* "A Noise Optimization Formulation for CMOS Low-Noise Amplifiers With On-Chip Low-Q Inductors" Ieee Transactions On Microwave Theory And Techniques, Vol. 54, No. 4, April 2006.

[10] T. H. Lee*, "The Design of CMOS Radio-Freqency Integrated Circuits"* 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2004