Analysis of power efficient SRAM cell for portable devices

Swaroop Kumar K, ShabirAhmed B J, Narendra K, Asha G H

***Abstract*—Static random-access memory (SRAM) is a type of semiconductor memory that uses bi stable latching circuitry to store each bit. SRAM exhibits data reminiscence but it is still volatile. In the early days of design, efforts were focused on optimizing the speed to address real-time problems. But Customers need devices with long battery life with more features supported. So the total power consumption should be reduced. Power consumption is of two types- Static and dynamic. Static power is the power dissipated in a design in the absence of any switching activity. The absolute and the relative contribution of leakage power to the total system power is expected to further increase in future technologies because of the exponential increase in leakage currents with technology scaling. The International Technology Roadmap for Semiconductors (ITRS) predicts that leakage power would contribute to 50% of the total power in the next generation processors. SRAMs are widely used in high-performance processors in the form of caches (tag and data arrays), branch target buffers, reservation stations, etc. Expectedly, SRAMs also contribute to majority of the leakage power in processors.**

Techniques like sleep approach, stack approach, sleepy stack, leakage feedback, leakage feedback with stack, sleepy keeper, sleepy keeper with stack, dual sleep, dual stack, variable body biasing are used to reduce leakage power. Each technique provides an efficient way to reduce leakage power. Dynamic power during write operation is reduced using 8T SARM cell design. Average power consumption of SRAM cell in each technique is obtained using both schematic and layout editor by MICROWIND at 65nm with a supply voltage of 1V at27^0C. At the end, comparison is made between all the foresaid techniques with the conventional 6T SRAM cell.

***Index terms*- sub threshold leakage current, dual sleep, sleepy stack, leakage feedback, sleepy keeper with stack, average power.**

I. INTRODUCTION

SRAM is more expensive and less dense than DRAM and is therefore not used for high-capacity, low-cost applications such as the main memory in personal computers. A typical SRAM cell is made up of six MOSFETs. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters.

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Two additional access transistors serve to control the access to the storage cell during read and write operations. Access to the cell is enabled by the word line which controls the two access transistors which in turn, control whether the cell should be connected to the bit lines: BL and logical NOT of BL. The symmetric structure of SRAMs also allows for differential signaling, which makes small voltage swings more easily detectable.

The power consumption of SRAM varies widely depending on how frequently it is accessed; it can be as power-hungry as dynamic RAM, when used at high frequencies. On the other hand, static RAM used at a somewhat slower pace, draws very little power and can have nearly negligible power consumption when sitting idle. Power dissipation which was previously considered an issue only in portable devices is rapidly becoming a significant design constraint in many system designs. Dynamic power has been a predominant source of power dissipation till recently. However, static power dissipation is becoming a significant fraction of the total power because of technology scaling. Static power is the power dissipated in a design in the absence of any switching activity and is defined as the product of supply voltage and leakage current. The absolute and the relative contribution of leakage power to the total system power is expected to further increase in future technologies because of the exponential increase in leakage currents with technology scaling. The International Technology Roadmap for Semiconductors (ITRS) predicts that leakage power would contribute to 50% of the total power in the next generation processors. Therefore, it is important for system designers to get an early estimate of leakage power to meet the challenging power constraints [7].

II. POWER REDUCTION TECHNIQUES

The increase in the functionality and performance of an integrated circuit with high density leads to feature technology scaling and reduction in threshold voltage. In order to maintain the actual characteristics of MOSFET the power supply voltage is also being reduced. This scaling leads to reduction in threshold voltage of the device and exponential rise in its leakage power consumption.

$$I_{subth} = A \times e^{\frac{q}{nkT}(V_{GS}-V_t)}\left(1 - e^{\frac{q V_{DS}}{kT}}\right) \ldots\ldots\ldots (1)$$

Technology scaling reduces the gate oxide thickness and the gate length thereby increasing the transistor density and also reduces the delay. Reduced gate lengths result in an increase in the leakage power dissipation. Increased transistor densities result in an increase in the power dissipation per unit area thereby creating hotspots. Scaling down the supply voltage reduces the switching power dissipation. Threshold voltage is

simultaneously scaled down along with the supply voltage significantly increasing the leakage power dissipation.

The total power in a CMOS is given by

$$P_{total} = P_{static} + P_{shortcircuit} + P_{dynamic} \quad \ldots. (2)$$

Where,

$$P_{static} = V_{DD} \times I_{leakage} \quad \ldots. (3)$$

And,

$$P_{shortcircuit} = V_{DD} \times I_{sc} \quad \ldots. (4)$$

$$P_{dynamic} = \frac{(\text{percentage activity} \times C_{total} \times V_{DD}^2)}{t_p} \quad \ldots. (5)$$

Base approach generally indicates conventional 6T SRAM cell. A typical SRAM cell is made up of six MOSFETs. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. Two additional access transistors serve to control the access to the storage cell during read and write operations. The pull-up network consists of only P-MOS transistors and pull-down network consists of only N-MOS transistors. It is a fundamental approach used generally in all other techniques.

The well-known traditional approach is the sleep approach [1] [2]. In sleep approach, an additional "sleep" PMOS transistor is placed between VDD and the pull-up network of the circuit and an additional "sleep" NMOS transistor is placed between the pull-down network and GND. These sleep transistors turn off the circuit by cutting off the power supply rails. Figure 2 shows its structure. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively. However, output will be in floating state after sleep mode, so the technique results in destruction of state plus a floating output voltage. These types of techniques are also called as Gated-VDD and Gated- GND [1].

Furthermore, the pull-up and pull-down networks will have floating values and thus will lose state during sleep mode. These floating values significantly impact the wake up time and energy of the sleep technique due to the requirement to recharge transistors which lost state during sleep.

Dual sleep approach takes the advantage of using the two extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. In OFF or ON state each of the pull-up and pull-down networks consists of both PMOS and NMOS transistors in order to reduce the leakage power. Figure 3 shows its structure. Advantages are- Firstly, it maintains state in sleep mode. Secondly, like the sleep, sleepy stack and sleepy keeper approaches, dual-V_{th} technology can be applied in dual sleep approach to get further reduction in leakage power [6].

Another technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor into two half sized transistors [1] [2]. Figure 4 shows its structure. When the two transistors are turned off together, induced reverse bias between the two transistors results in sub threshold leakage current reduction. However, divided transistors increase delay significantly and could limit the usefulness of the approach.

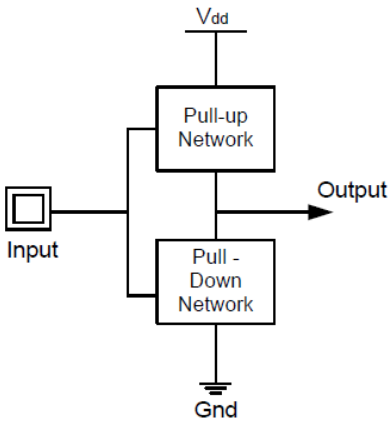

Fig 1: Base approach

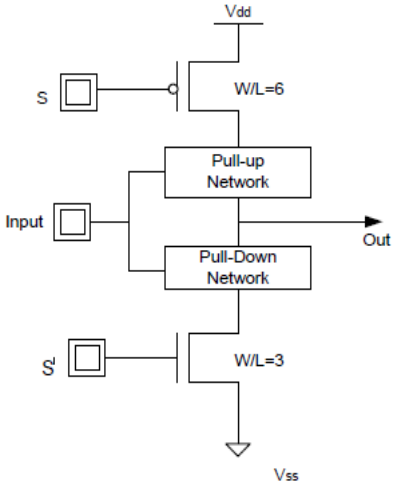

Fig 2: Sleep approach

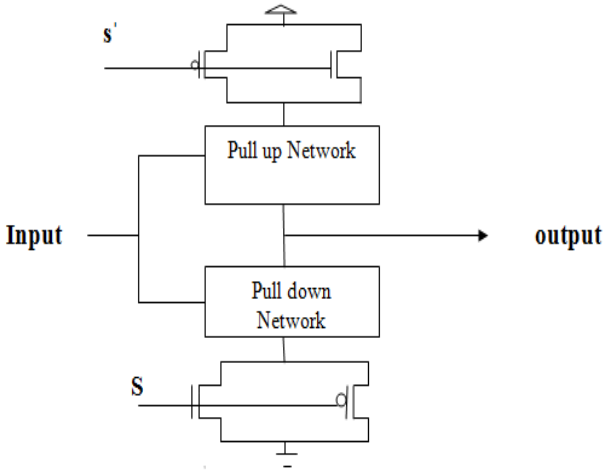

Fig 3: Dual sleep approach

The dual stack approach uses two extra PMOS in the pull down network and two extra NMOS in the pull up network. As a result the NMOS degrades high logic level and the PMOS degrades the low logic level. Figure 5 shows its structure. Due to the body effect they further decrease the voltage level. So, the pass transistor decreases the voltage applied across the main circuit. The stacked transistors are held in reverse body bias. As a result their threshold is high.

High threshold voltage causes low leakage current and hence low leakage power.

The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors [1] [2]. Figure 6 shows its structure. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active mode. However, area penalty is a significant matter for this approach since every transistor is replaced by three transistors and since additional wires are added for S and S', which are sleep signals.

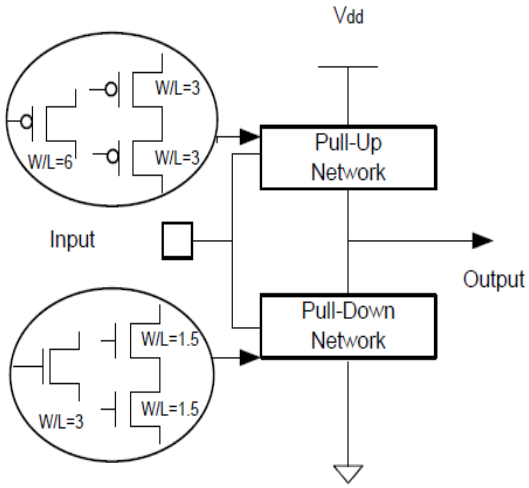

Fig 4: Stack approach

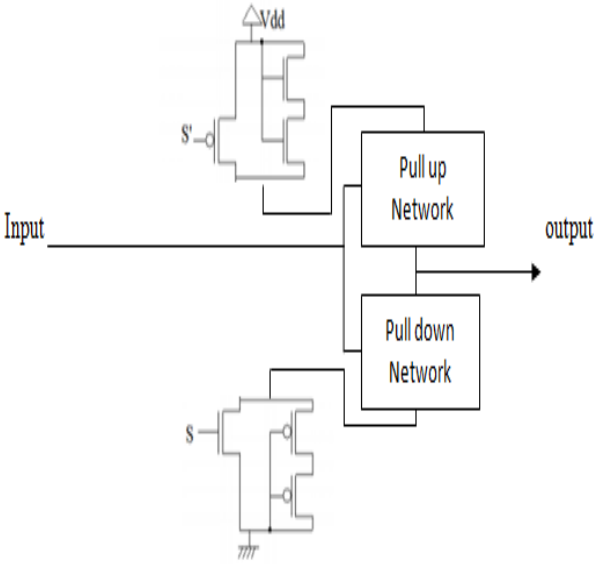

Fig 5: Dual stack approach

The leakage feedback approach is based on the sleep approach. However, the leakage feedback approach uses two additional transistors to maintain logic state during sleep mode, and the two transistors are driven by the output of an inverter which is driven by output of the circuit implemented utilizing leakage feedback [1] [2] .

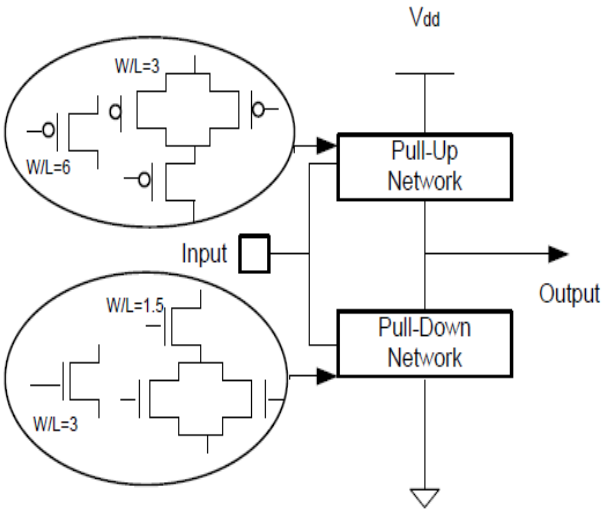

Fig 6: Sleepy stack approach

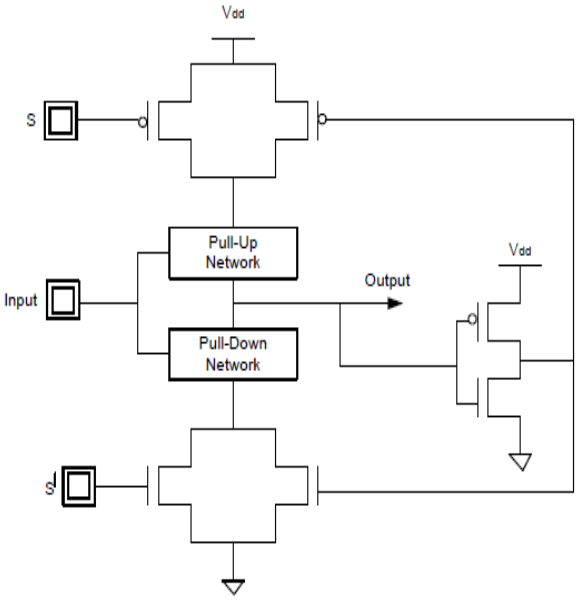

Fig 7: Leakage feedback approach

Traditionally the CMOSFETs are used only in their most efficient, and naturally inverting, way: i.e.., PMOS transistors are connected to VDD and NMOS transistors are connected to GND. It is well known that PMOS transistors are not efficient at passing GND; similarly, NMOS transistors are not efficient at passing VDD. However, to maintain a value of 1 in sleep mode, given that the "1" value has already been calculated, the sleepy keeper approach uses this output value of"1" and an NMOS transistor connected to VDD to maintain output

value equal to "1"when in sleep mode[1] [8].Figure 8 shows its structure.

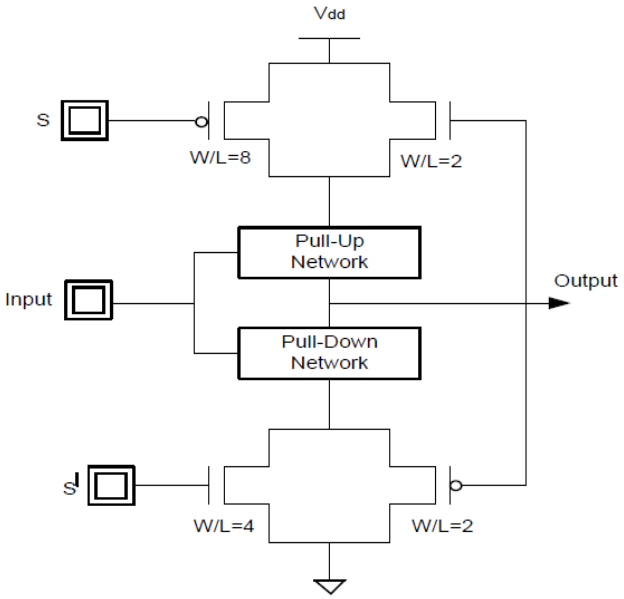

Fig 8: Sleepy Keeper approach

Leakage feedback with stack (LFS) technique combines the two low power techniques i.e. leakage feedback approach due to less transistors than sleepy-stack and ultra-low power technique i.e. Stack approach [9].Figure 9 shows its structure.

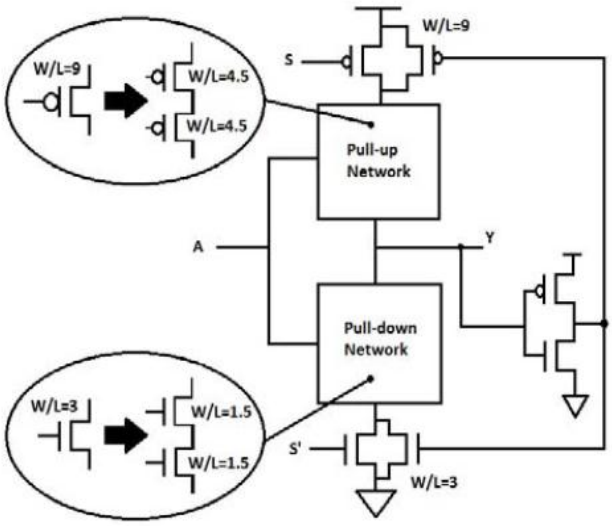

Fig 9: Leakage feedback with stack approach

Sleep stack with keeper (SSK) combines three leakage power reduction techniques i.e. sleep technique, stack technique with keeper technique. It is one of the best power reduction technologies along with leakage feedback with stack approach where the average power consumption is almost negligible i.e. in nano watts [9]. Figure 10 shows its structure.

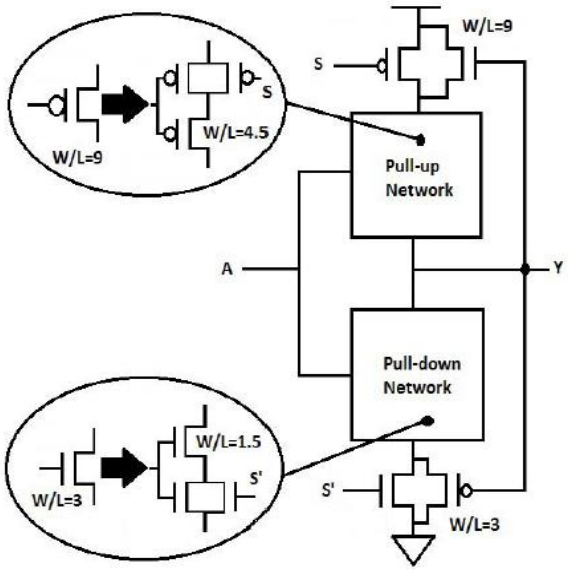

Fig 10: Sleepy keeper with stack approach

Charging and Discharging of Bit Lines consume more power during the Write "1" and Write "0" operation. Since Write operation consumes considerable larger power due to the full voltage swing on the bit-lines than read operation, emphasis is given to reduce dynamic power consumption during write operation. In this method SRAM cell includes two more trail Transistors in the pull down path for proper charging and discharging of Bit Lines [3] [5]. Figure 11 shows the structure of 8T SRAM.

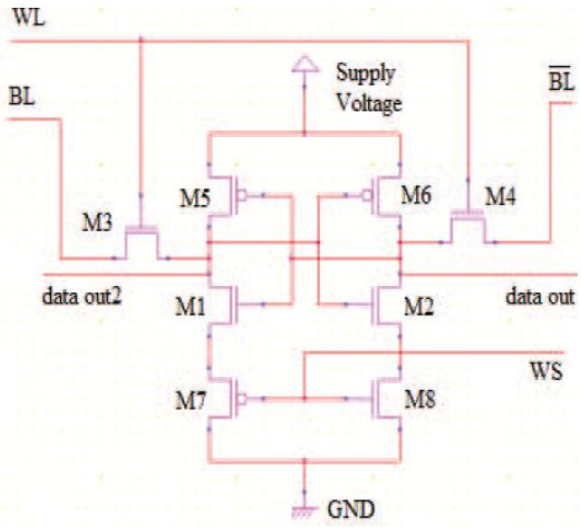

Fig 11: 8T SRAM cell

In write "1" mode, BL is set to "0" and then the word line is asserted. In write "0" mode, BL is set to "1" and then the word line is asserted. The WS signal is used to ensure the correct operation and by selecting proper value of signal WS before asserting WL, transition from 1 - 0 and 0 - 1 can be easily allowed. In order to reduce the sub threshold current which is flowing in the circuit when transistor is in Cut Off region the two pull down transistors are used. This leakage current is dependent on Threshold Voltage. As the threshold voltage decrease the Sub-threshold current increases.

III. RESULTS

The conventional 6T SRAM cell and all the remaining techniques are drawn DSCH3 schematic editor. The DSCH program is a logic editor and simulator. DSCH is used to validate the architecture of the logic circuit before the microelectronics design is started. The verilog files are created for each schematic and are compiled in MICROWIND to get the actual layout at the physical level at 65nm and at a supply voltage of 1V.The MICROWIND program allows designing and simulating an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate.

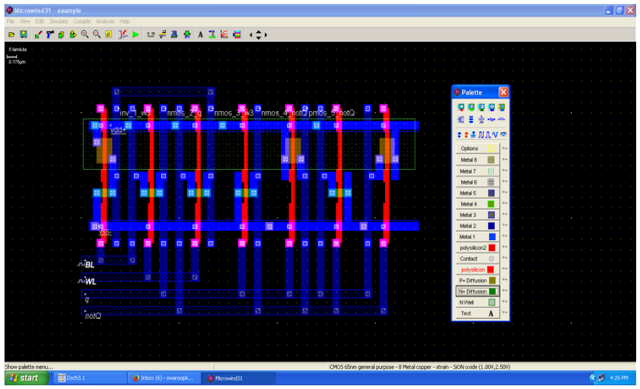

Fig 12: Layout of 6T SRAM (Base approach)

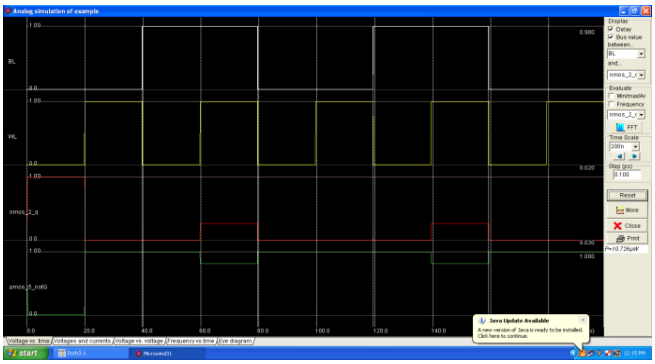

Fig 13: Simulation result for 6T SRAM

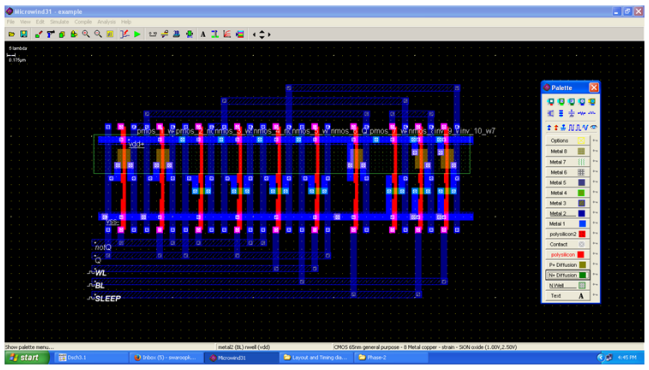

Fig 14: Layout of 6T sleep SRAM cell

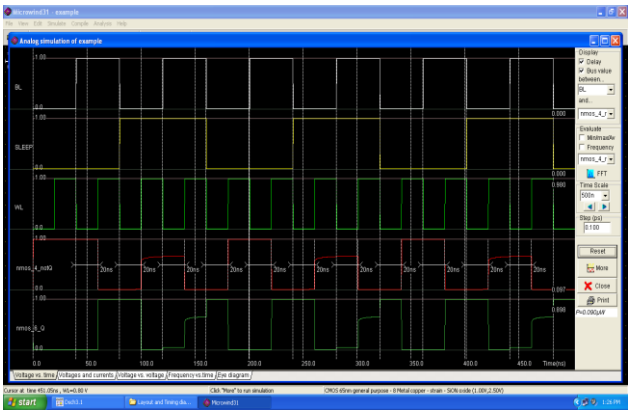

Fig 15: Simulation result for 6T Sleep SRAM

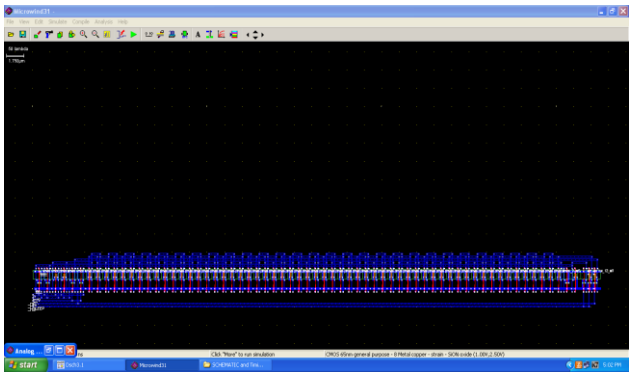

Fig 16: Layout of 6T Dual sleep SRAM cell

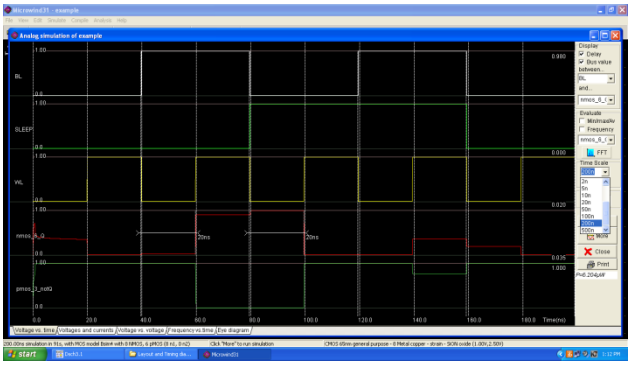

Fig 17: Simulation result for 6T Dual sleep SRAM

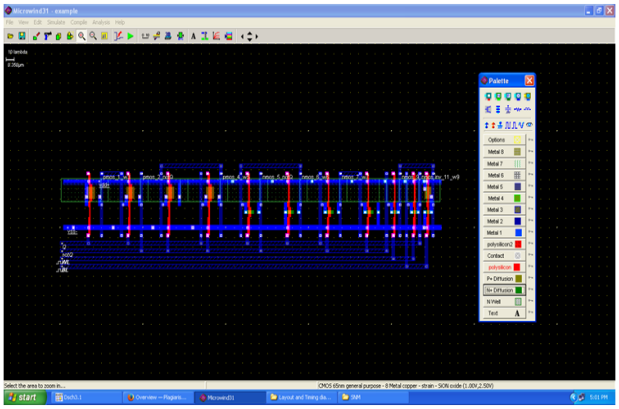

Fig 18: Layout of 6T Stack SRAM cell

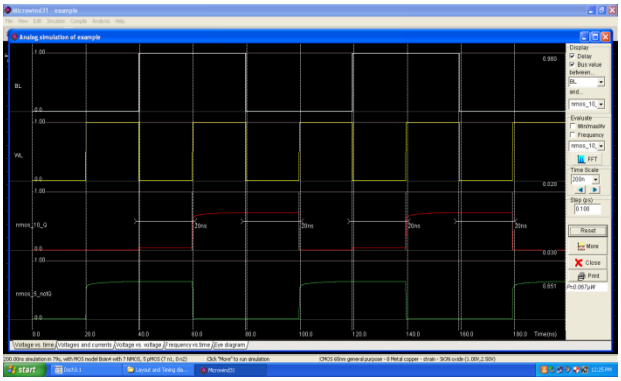

Fig 19: Simulation result for 6T Stack SRAM

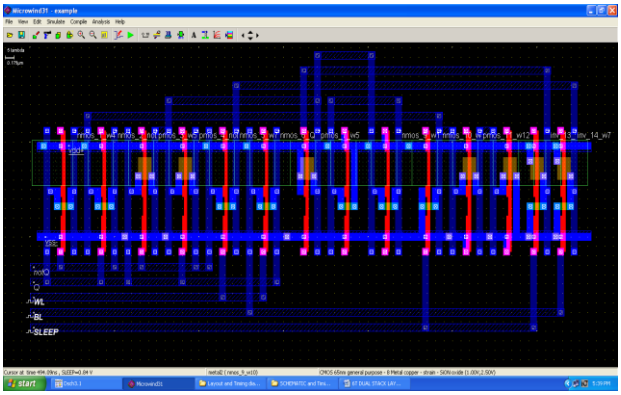

Fig 20: Layout of 6T Dual Stack SRAM cell

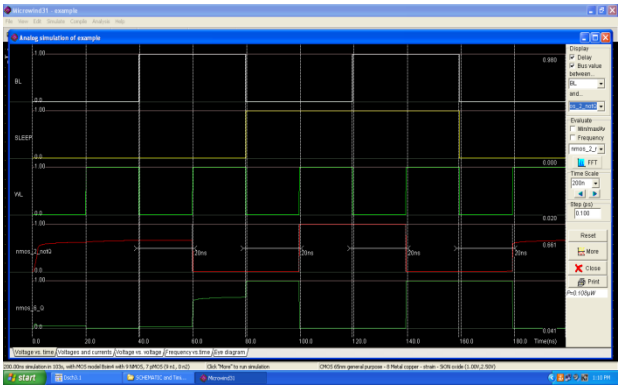

Fig 21: Simulation result for 6T Dual Stack SRAM

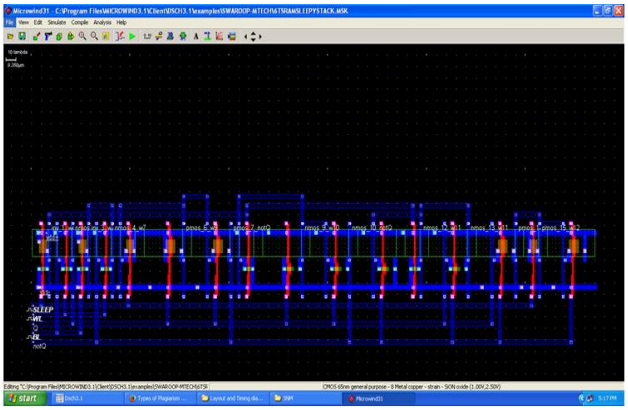

Fig 22: Layout of 6T Sleepy stack SRAM cell

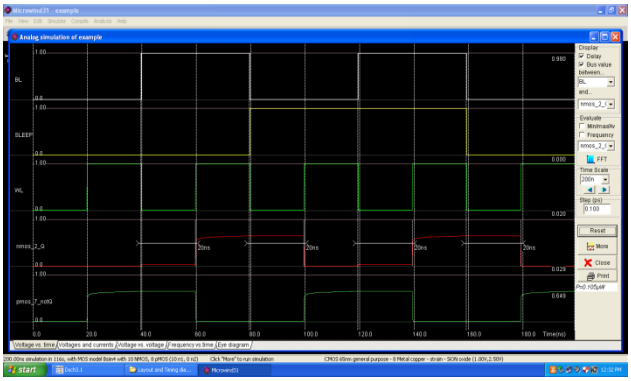

Fig 23: Simulation result for 6T Sleepy stack SRAM

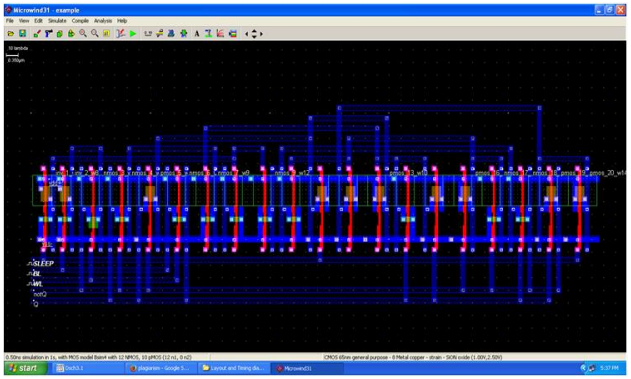

Fig 24: Layout of 6T Leakage feedback SRAM cell

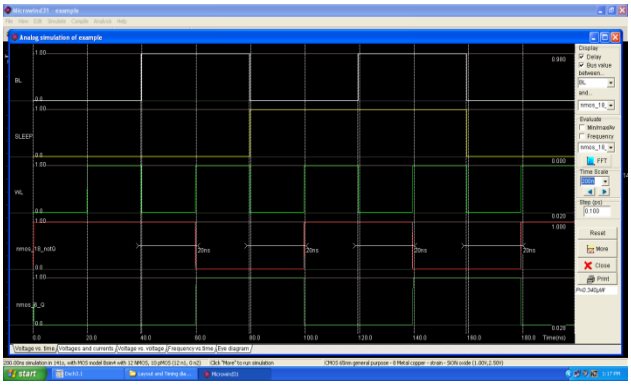

Fig 25: Simulation result for 6T Leakage feedback SRAM

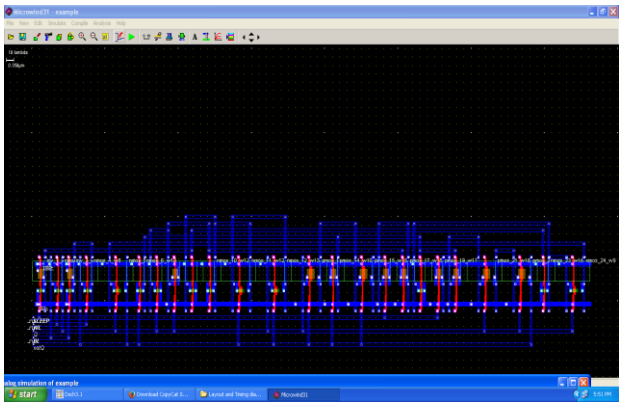

Fig 26: Layout of 6T LFS SRAM cell

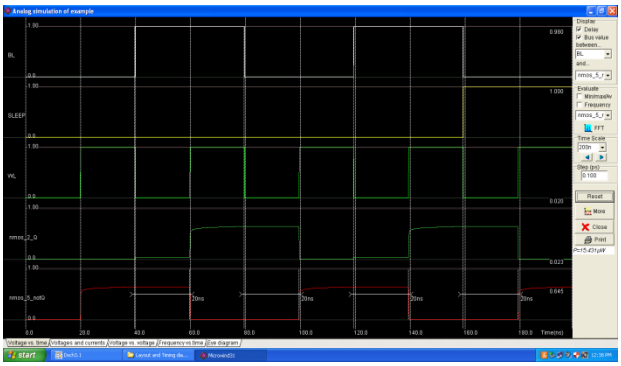

Fig 27: Simulation result for 6T LFS SRAM

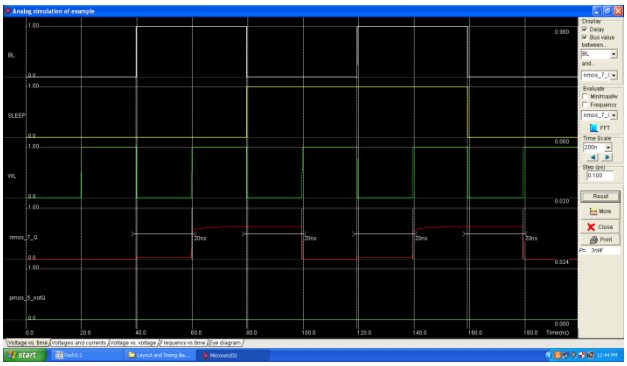

Fig 31: Simulation result for 6T SSK SRAM

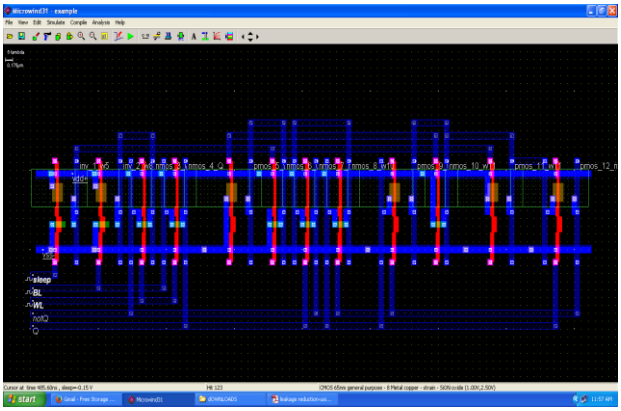

Fig 28: Layout of 6T Sleepy keeper SRAM cell

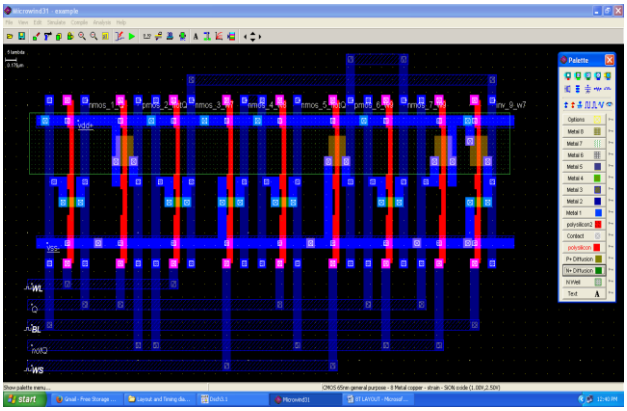

Fig 32: Layout of 8T SRAM cell

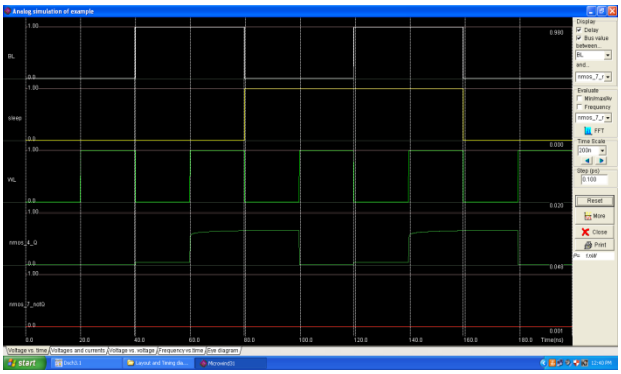

Fig 29: Simulation result for 6T Sleepy

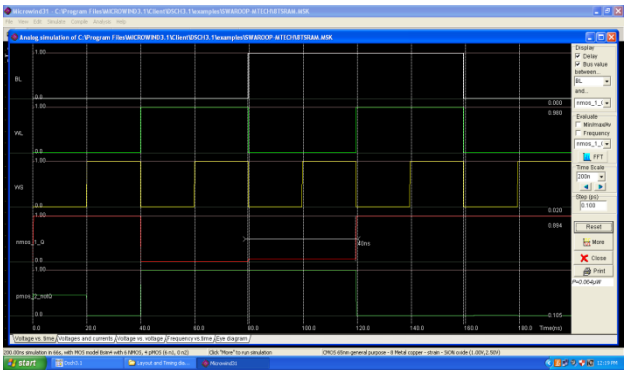

Fig 33: Simulation result for 8T SRAM

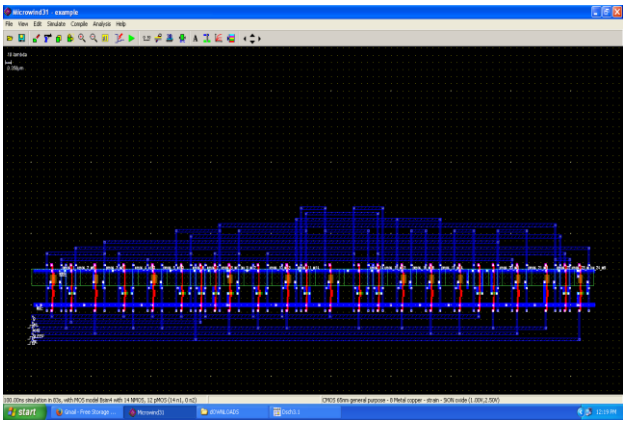

Fig 30: Layout of 6T SSK SRAM cell keeper SRAM

Table1, table 2and table 3 gives the average power consumption of the above discussed techniques at different frequencies with a supply voltage of 1V at 27^0C.

Table 1: Average power consumption

Frequency (Hz)	6T SRAM (µw)	6T SLEEP (µw)	6T DUAL SLEEP (µw)	6T STACK (µw)
2M	12.828	0.090	6.984	0.056
5M	10.726	0.105	6.204	0.067
10M	10.780	0.119	1.221	0.056
50M	0.250	0.345	5.745	0.059
100M	0.471	0.688	11.489	0.101
500M	2.349	3.439	57.436	0.504
1G	4.697	6.877	0.108	1.008

Table 2: Average power consumption

Frequency (Hz)	6T DUAL STACK (µw)	6T SLEEPY STACK (µw)	6T LEAKAGE FEEDBACK (µw)	6T LFS (µw)
2M	0.101	0.080	0.294	16.244
5M	0.108	0.105	0.340	15.431
10M	0.097	0.107	0.355	13.611
50M	0.314	0.297	1.174	0.586
100M	0.618	0.576	2.346	1.154
500M	2.794	2.878	11.723	5.765
1G	4.801	5.756	23.445	11.529

Table 3: Average power consumption

Frequency (Hz)	6T SLEEPY KEEPER (µw)	6T SSK (µw)	8T SRAM (µw)
2M	1nW	1nW	0.057
5M	1nW	3nW	0.064
10M	2nW	7nW	0.086
50M	0.010	0.020	0.226
100M	0.010	0.020	0.450
500M	0.099	0.099	2.234
1G	0.197	0.197	4.453

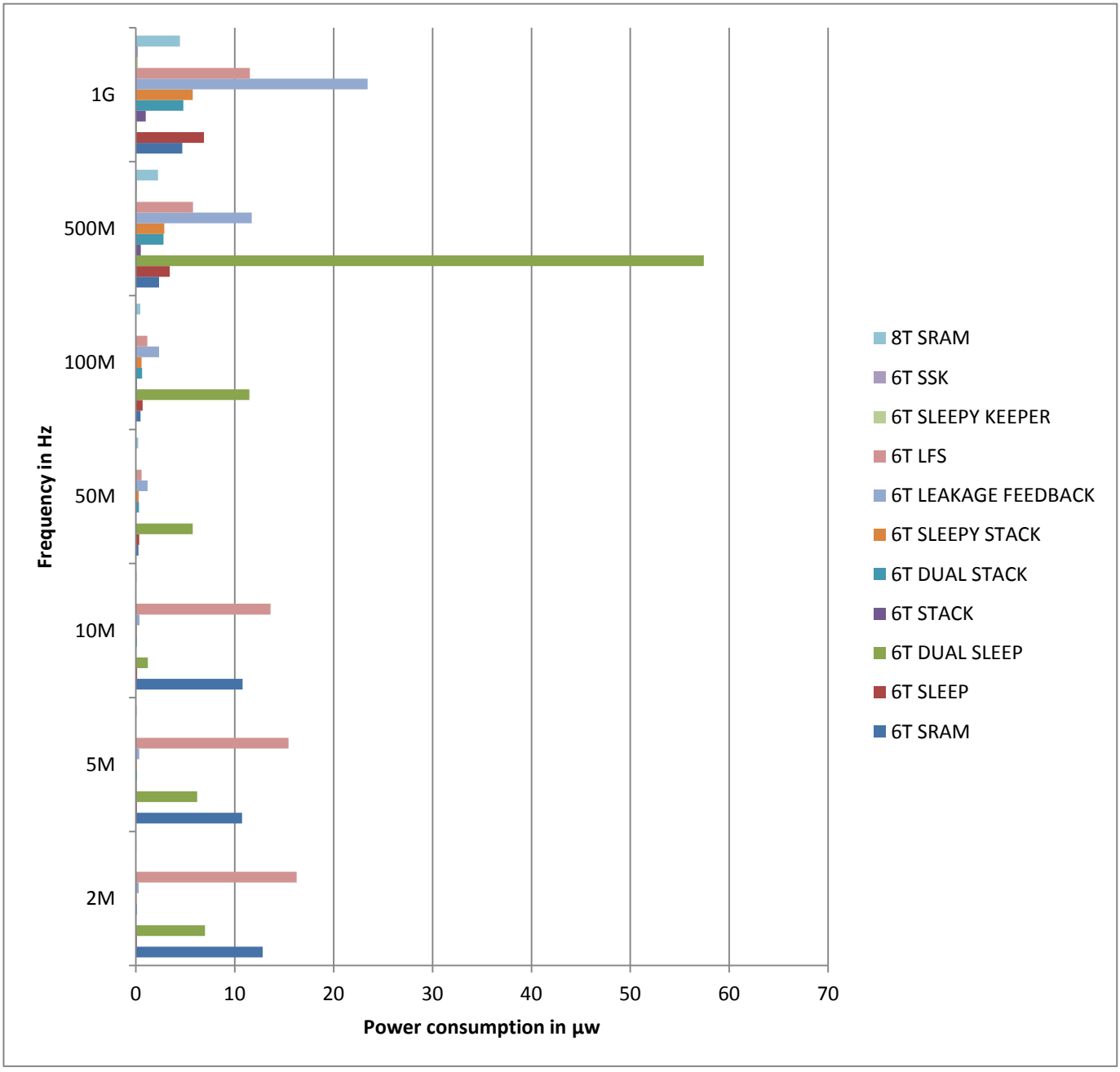

Fig 34: Graph of Average power consumption

IV. CONCLUSION

According to the report of ITRS, it is necessary to reduce the leakage power in memory circuits as it will going to be the prime contributor to the total power dissipation in coming years. So there are many approaches as discussed above which reduce the leakage power to different extents at the cost of area and delay. Among the discussed techniques, stack, sleepy keeper, sleepy keeper with stack and 8T SRAM are good candidates when compared to others. Although number of transistors is increased, relative power dissipation reduces considerably. Area efficient memory of dimension 4K, 16K and higher can be implemented using these low power SRAM cells. The choice of selecting a particular technique depends on particular application.

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