

# Design of Low Power & Reliable Networks on Chip through Joint Crosstalk Avoidance and Multiple Error Correction Coding

Padmini G. Kaukshik, Neha Santosh Parihar, Pranoti B.Patil

**Abstract**— Achieving reliable operation under the influence of deep-submicrometer noise sources including crosstalk noise at low voltage operation is a major challenge for network on chip links.

In this seminar, a coding scheme is presented that simultaneously addresses crosstalk effects on signal delay and detects up to seven random errors through wire duplication and simple parity checks calculated over the rows and columns of the two-dimensional data. This high error detection capability enables the reduction of operating voltage on the wire leading to energy saving.

The results show that the proposed scheme reduces the energy consumption up to 53% as compared to other schemes at iso-reliability performance despite the increase in the overhead number of wires. In addition, it has small penalty on the network performance, represented by the average latency and comparable codec area overhead to other schemes.

**Index Terms**— Plasma antenna; Keywords Network on Chip . Crosstalk avoidance . Multiple error correction. Low power. Transient errors .Joint codes

## I. INTRODUCTION

Transmission Network on chip (NoC) is a set of small routing components connected by relatively short wires which has been proposed as the main solution for communication between the many blocks in a monolithic chip replacing the long traditional buses[1][2]. This becomes indispensable for chip integration scalability as more blocks are integrated in a single chip due to the continuous scaling down of semiconductor technology. One of the major challenges in NoC is the communication reliability due to the small feature sizes, high operating frequency and low operating voltage of the chips. Faults affecting semiconductor devices can be classified as permanent, intermittent and transient faults , which negatively impact NoCs communication reliability[3]. Permanent faults are irreversible changes due to manufacturing defects or device wearout. Under temperature and voltage variations, hardware instabilities may result into intermittent faults manifesting as burst of errors that repeatedly occur in same locations Transient faults can be caused by several noise sources such as crosstalk noise, power

supply noise, alpha particles, electromagnetic interference (EMI) and transistor variability .Faults affecting the links result in incorrect interpretation of the data and/or control signals and are usually addressed using error detection/correction coding such as simple parity or Hamming codes[6,7].

Crosstalk noise has posed as one of the most challenging problems in timing closure and power consumption of modern VLSI circuits. Short wire spacing and high aspect ratio of the interconnects in deep- sub micrometer processes increase the coupling capacitance and in turn affects the integrity and timing of signals and contributes to the increase of interconnect power consumption[3,5,8]. To address the crosstalk and other transient fault noise sources simultaneously, researchers have proposed joint error correction/detection note that CAC reduces the bus power consumption through the reduction of adjacent wire switching activity .The joint code proposed in pointed out that there is diminishing return in power reduction when error correction capability exceeds four errors. This observation could be valid for systems with low noise deviations. For systems with high noise deviations, it is possible to achieve larger power saving by adopting higher error detection/correction capabilities schemes .In this paper, we propose a new joint coding scheme that can detect up to seven errors and simultaneously reduce the crosstalk effect through duplication, as opposed to previous works that achieve up to only 4 errors detection. The encoding scheme is based on parity codes generated by arranging the data into two-dimensional arrays and calculating the parity for each independent row and column and finally duplicating all the bits. In order to achieve high detection capability, the two copies of each bit are compared in addition to checking the parities at the decoder.

## II. LITERATURE REVIEW

Several error detection/correction schemes for NoC environments were proposed. Cyclic Redundancy Check (CRC), simple parity and Hamming codes were analyzed for the NoC environment [6,7,18].The use of orthogonal latin square codes was proposed in to provide up to four error correction capability. the authors proposed the usage of multiple groups of Hamming codes to provide higher error detection and correction. The drawback of this scheme is that it is not able to detect more than two random errors in each group.

The authors proposed the use of type-II Hybrid Automatic Repeat Request (HARQ) scheme where only the rows codes are sent in the first transmission and the rest of the check bits are sent if uncorrectable errors are detected. Despite its

Manuscript received January 18, 2015.

Padmini G. Kaukshik, Professor in EXTC Department, Jawaharlal Darda Institute Of Engineering And Technology, Yavatmal,India

Neha Santosh Parihar, Final Year (EXTC) Student, Jahawarlal Darda Institute Of Engineering And Technology, Yavatmal,India

Pranoti B.Patil, Final Year (EXTC) Student, Jahawarlal Darda Institute Of Engineering And Technology, Yavatmal,India.

capability of detecting/correcting multiple errors, it could not detect/correct more than two errors for any row.. It is worth mentioning here that these schemes addressed the transient fault noise sources excluding the crosstalk noise on signal delay. This works addressed the timing effects of crosstalk, however they did not provide fault tolerance against other sources of transient fault noise. Some techniques include shielding, repeater insertion and skewed transitions.

To simultaneously achieve crosstalk-based timing reduction and single error correction capability, Duplicate-Add-Parity (DAP) code was proposed by duplicating the data bits and adding one parity bit [3]. On the other hand, DAPX, a modification of DAP, duplicated the parity bit to reduce the crosstalk delay effect on this particular bit. Other schemes which have similar correction capability and addressed crosstalk through duplication approach are the Dual Rail (DR), Boundary Shift Code (BSC) and Modified Dual Rail code (MDR). These schemes have simple codec but are limited by the correction of only single errors.

Triplication coding with green bus encoding alongside with voltage scaling was proposed in [8]. However due to its single error correction in a group of three bits, slight decrease in the voltage swing can be achieved as compared to DAP. Note that, in the ultra deep submicrometer (UDSM) technology, multiple errors are expected to occur and thus single error correction capability will not be sufficient. Crosstalk aware multi-bit error detection/correction codes were proposed, in double error correction was achieved through joint crosstalk avoidance and double error correction code (CADEC) scheme. The scheme proposed to encode the data using Hamming single error correction code and then encode the resulting check bits and the data bits using DAP approach. This idea was extended to triple error correction in joint crosstalk avoidance and triple error correction (JTEC) code and extended to quadruple error detection in JTEC with simultaneous quadruple error detection (JTEC-SQED) code. The increased error detection/correction allows the links to operate at lower voltage swing to reduce the power consumption while achieving the required reliability.

In this seminar, a new coding scheme is proposed that combines two dimensional parities with duplication to jointly provide high error detection and crosstalk avoidance capability. This joint scheme achieves up to seven random errors detection in which the high detection capability is not limited to address burst errors. This allows for further reduction in the voltage swing with respect to previous works, leading to higher energy savings.

### III. CODING IN NOCS

A few NoC interconnect architectures have been proposed by different research groups. Figure shows two of the most commonly used NoC architectures. Data exchange between the functional blocks takes place in the form of packets. Generally, wormhole switching is adopted for. This scheme divides packets into fixed-length flow control units (flits), with I/O buffers storing only a few flits. The first flit, i.e., header flit, of a packet contains routing information. Header flit decoding enables the switches to establish the path and subsequent flits simply follow this path in a pipelined fashion. The delay of an inter-switch wire in the NoC link depends on the transitions on the wire and wires adjacent to it. The worst

case delay of a wire  $(1+4\lambda)f$  is where  $f$  is the delay of a crosstalk-free wire and  $\lambda$  is the ratio of the coupling capacitance to the bulk capacitance.

FIGURE I.(a)mesh (b)torus based NOCs

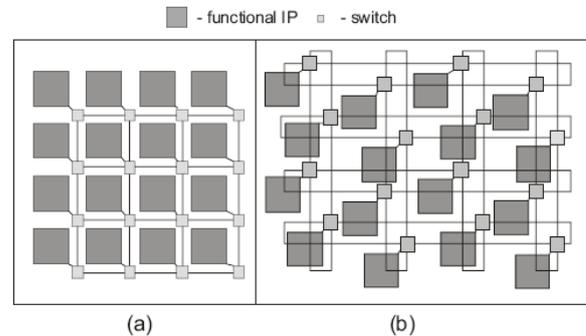


Figure 1: (a) Mesh; (b) Torus-based NoCs

The purpose of the crosstalk avoidance code is to reduce the delay of the line to  $(1+P\lambda)f$  where  $p=1, 2, \text{ or } 3$  is called the maximum coupling. As a result of reduction in the coupling capacitance, the CACs will reduce the energy dissipation per line in a NoC link.

### IV. ERROR CORRECTION CODING SCHEME

In general, it is possible to achieve higher error detection than correction with the same amount of redundancy since a block code with Hamming distance,  $D$  can detect up to  $(D-1)$  errors while it can correct only  $\lfloor (D-1)/2 \rfloor$  errors. However, the drawbacks of the error detection schemes are the communication latency and energy consumption imposed by the retransmissions. Despite these disadvantages, In this we demonstrate that with precise selection of the voltage swings of the links, the performance and energy consumption of the NoC will not be highly impacted by the retransmission

#### A. DUPLICATED TWO-DIMENSIONAL PARITIES (DTDP) Scheme(DTDP)

This coding scheme is designed based on two principles: wire duplication to reduce crosstalk effect on signal delay and two-dimensional parities to provide error detection. By arranging the data in a two-dimensional matrix and calculating the parity for each row and column, the equals to 4. This configuration allows the possibility to correct one error and detect up to two errors, or to detect 3 errors without any error correction capability. Through wire duplication, the scheme achieves twofold objective. First, the crosstalk effect on signal delay manifested in CIBD can be reduced through the reduction of effective coupling capacitance. Second, the duplication doubles the to 8, which leads to a maximum of seven random errors detection (7ED) capability. Despite the increase in the number of wires, this report it shows that the energy saving through the wire supply voltage reduction

exceeds the energy consumed by the additional wires under isoreliability performance.

**B. DTDP-7ED ENCODER**

Fig.2 shows the encoding process where the K data bits are arranged in R rows and C columns and then parities are calculated for each rows and columns respectively. Row parity

Can be defined as  $PR_Q = B_{QC} \oplus B_{QC+1} \oplus \dots \oplus B_{QC+C-1}$  for  $Q = 0$  to  $R-1$ , column parity  $PC_Q$  can be defined as  $PC_Q = B_{Q0} \oplus B_{Q+C} \oplus \dots \oplus B_{Q+(R-1)}$  for  $Q=0$  to  $C-1$ .The resultant codeword is duplicated before being sent over the link.The duplication produces  $2 \times (C+1)$  and  $2 \times (R+1)$  codeword bits per row and column respectively as shown in fig.(a).Fig(b) shows the encoder implementation .

FIG.II. DTDP-7ED encoder

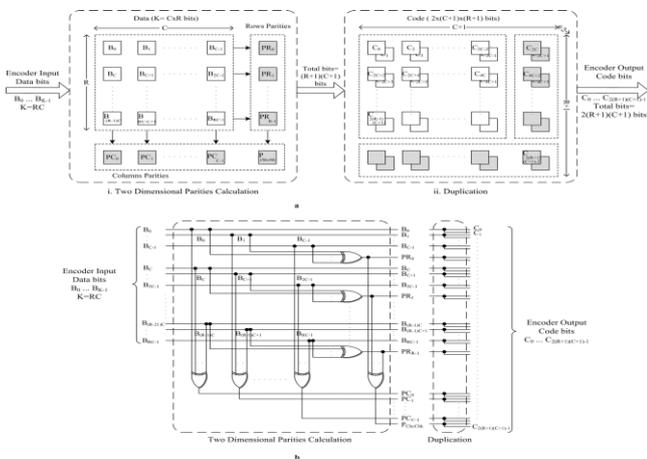


Fig. 1(b) shows the encoder implementation. It can be noticed that the critical path delay is the generation as it takes the rows parities as inputs to its XOR chain. Since the proposed coding scheme is based on ARQ error control policy, it requires a retransmission buffer and retransmission request signal coming from the decoder. For simplicity reason, they are not shown here in this figure. Note that upon receiving retransmission request, the encoder encodes the data in the retransmission buffer instead of the new data. The selection of and of the data arrangement matrix affects the codeword size before duplication,CW , where CW = K+R+C+1.

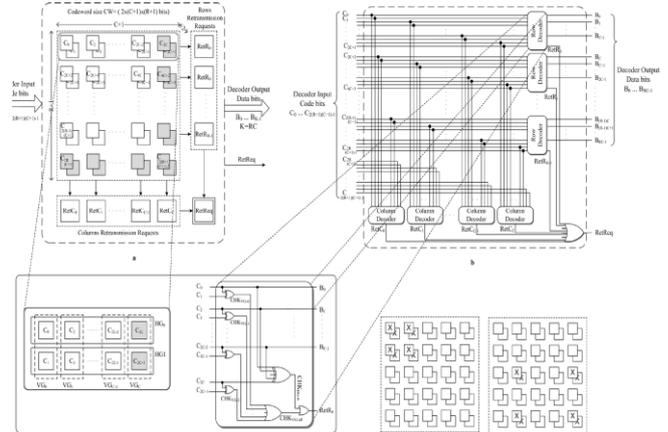
**C. DTDP-7E DECODER**

As Fig. 3(a) shows, the codeword bits received are arranged in a two-dimensional matrix similar to the two-dimensional matrix after duplication in the encoding process with R+1 rows and columns C+1. The decoding is applied to each row and column by calculating the parities to check for errors and generating the retransmission request signals,RetR andRetC for each individual row and column except the last row. The final retransmission requestRetReq is set when at least oneRetR or oneRetC signal is set. TheRetReq signal is also used to indicate to the next stage in the router pipeline the validity of the decoder output data.

Decoder implementation in Fig. 3(b) shows that the signal and output data bits are generated by the row decoder block Q while the column decoder block Q generates the RetCqsignal. Note that both row and column decoder blocks have similar

implementations, therefore, to illustrate the decoding mechanism.

FIG.III.DPTR 7E decoder



**V. RELIABILITY**

**A. BIT RATE ERROR:**

The bit rate error (BER), can be represented using the Gaussian noise model, with zero mean ,σ<sub>N</sub><sup>2</sup> is the variance of noise source and Vsw is the voltage swing on the wires. The BER can be given by:

$$\epsilon = Q \left( \frac{V_{sw}}{2\sigma_N} \right)$$

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^\infty e^{-\frac{y^2}{2}} dy$$

The reduction of Vsw reduces the power consumed in the links. However ,at any noise level, ε increases with the reduction of Vsw and the model in accounts for decrease in noise margin due to reduced voltage swing This increases the probability of flit errors resulting in lower reliability. One possibility to compensate the low reliability is through the use of error detection or correction codes. These codes will require encoder and decoder in addition to extra wires for the check bits which form the overhead power consumption that should be minimized. It was shown in [6], [12] that by reducing , quadratic power saving on the links can be achieved surpassing the overhead power consumption, resulting in overall power saving.

**B. UNDETECTABLE ERROR PROBABILITY**

The undetected error probability, , is the probability that a flit has errors that cannot be detected by the error detection or correction scheme. Note that each scheme has different detection capability, thus has different undetected error probability model. For the case of uncoded flits, the is the same as the word error probability.

The probability to receive bits error free is(1-ε)<sup>L</sup> . The probability to have at least one erroneous bit in this bit word, defined as word error probability, can be given by  $P_{word\ error}(\epsilon) = 1-(1-\epsilon)^L$

**C. RETRANSMISSION PROBABILITY:**

Coding schemes with error detection and/or correction capabilities can be further categorized into one of the three error control policies: automatic repeat request (ARQ), forward error correction (FEC), or hybrid ARQ (HARQ). The

number of retransmissions for each coding scheme differs according to the adopted error control policy, causing different effect on the communication latency and energy.

A retransmission is requested when the decoder detects an error that cannot be corrected, therefore the flit retransmission probability of coding scheme X can be expressed by :

$$P_{ret-x} = P_{unc-x} - P_{und-x} \text{Type equation here.}$$

Where P<sub>unc</sub> is the probability that a flit has error(s) that cannot be corrected by the scheme's decoder and P<sub>und</sub> is the probability that a flit has undetected errors.

### VI. POWER AND CONSUMPTION

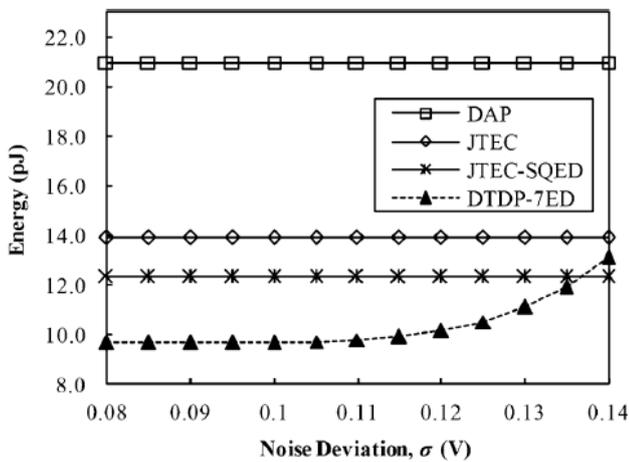
With the assumption of same router architecture implemented for all the coding schemes, the difference in power consumption comes from the encoder, decoder and links. Thus the average power p, can be given by:

$$P = P_{encoder} + P_{decoder} + P_{link}$$

$$P_{link} = (L \cdot C_L \cdot \alpha_{wire} + (L-1) \cdot C_c \cdot \alpha_c) \frac{1}{2} V^2 \cdot f$$

Where C<sub>L</sub> is the number of wires in the link, C<sub>c</sub> and are the self and coupling capacitance of wire and between wires respectively, α<sub>c</sub> and α<sub>wire</sub> are the wire self-transition and coupling transition activity factor respectively, V is the supply voltage and the operating frequency. The first term in the equation represents the link self switching power consumption, while the second term represents the link power consumption due to the coupling capacitance.

FIG.IV.Power And Consumption



### VII. ADVANTAGES OF DTDP SCHEME

- The error correction scheme DTDP, can detect upto 7 errors which ass compared to other error correction schemes.
- The error correction scheme, DTDP, ensures the high error correction capability enables the reduction of operating voltage on wire leading to energy saving.
- The results shows that the encoding reduces power consumption upto 53% as compared to other schemes at isoreliability performance despite the increase in the overhead number of wires.

### VIII. RESULT AND CONCLUSION

In this seminar , a crosstalk aware seven error detection coding scheme was proposed. The undetected error probability and retransmission probability of the proposed scheme were derived. The residual flit error probability, a representative of the schemes' reliability, was compared as a function of BER. The results show that the proposed scheme, DTDP-7ED, can achieve the same reliability under higher BER, allowing the link to work in lower voltage swing. The reduced voltage swing enabled DTDP-7ED to reduce the average power and energy consumptions as compared to the other schemes despite the increase in energy with the increase of noise due to retransmissions. It was shown that providing higher error detection brings energy savings when working in noisy environments. Furthermore, using ARQ error control policy with higher error detection achieves energy savings with relatively small impact on performance, highly suitable for medium to high reliability systems.

### IX. FUTURE SCOPE

This error detection/correction technique to investigate joint crosstalk avoidance and multiple error correcting codes and their performance in NoC fabrics .But this coding technique can detect upto only 7.This conclude that the minimum number of erros that causes the DTDP-7E decoding failure is eight. This suggests that higher order error correcting codes will be more area efficient than retransmission-based mechanisms.

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