Comparative Study and Analysis of Fast Multipliers

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***Abstract*— Fast multipliers are essential parts of digital signal processing systems.In recent electronics, with advances in technology, the power consumption, as well as delay and area has become the essential factors in VLSI design that limits the performance of any circuit. A multiplication is the basic mathematical operation which is present in many part of the digital computer especially in signal processing task, such as graphics and computation system, in high speed integrated circuits and application-specific ICs. This paper oriented to performance comparison of Booth scheme, Dadaa scheme and Wallace scheme in terms of multiplier,with characterize parameters-Area, delay and power . In this paper we have analyzed and reviewed that the Wallace tree multiplier has least power dissipation comparison of Booth and Dadda multiplier. Since power minimization is becoming very important for a number of reasons ranging from increasing demand for portable computing to the problem of hot chip due to increasing clock frequencies and device counters. Wallace tree multiplier is fastest among all the multipliers whereas Booth multiplier is a best choice when speed is not important. The design is implemented at 90 nm technology and Xilinx ISE tool is used for simulation.**

***Index Terms*- Power, area, partial product ,DSP, transistor digital Multipliers.**

I. Introduction of Multipliers

A multiplier is one of the key hardware blocks in most digital and high performance systems such as FIR filters, digital signal processors and microprocessors etc. With advances in technology our aim at offering higher speed and lower power consumption even while occupying reduced silicon area. This makes them compatible for various complex and portable VLSI circuit implementations. Power consumption has become a critical concern in today's VLSI system design. The growing market for fast floating-point co-processors, digital signal processing chips, and graphics processors has created a demand for high speed, area-efficient multipliers.In figure 1 Multiplication involves three main steps:

- Partial product generation
- Partial product reduction
- Final addition

The second stage of partial products reduction produce better performance and convenient design of the multiplier. An electronic computing unit used to provide multiplication processes at a very high speed. In digital design many type of multipliers like as series multipliers ,parallel multipliers Array multipliers, Booth multiplier, Dadda multiplier,Wallace Tree multipliers with different speeds, areas, and other configurations.

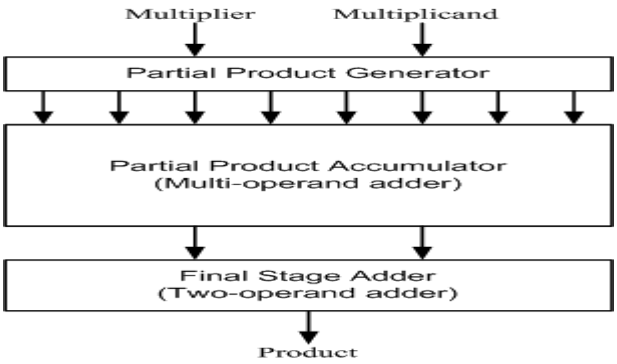

Figure 1. Basic block diagram of multiplier

The main aim is, to achieve partial product accumulated by successively reducing the number of bits of information in each column using full adders or half adders. By applying the basic three input adder in a recursive manner, any number of partial products can be added and reduced to two numbers without a carry propagate adder.

II. OVERVIEW OF MULTIPLIERS SCHEME

- The Booth scheme provides a simple way to generate the product of two signed bi-nary numbers. Booth multiplication algorithm is used in Booth multiplier. The total delay of booth multipliers is depend on the logarithm of the operand word length.
- The Dadda scheme essentially mini- mises the number of adder stages required to perform the summation of the partial products[12]. This is achieved by using full and half adders to reduce the number of rows in the matrix of bits at each summation stage.Its working is similar to that of Wallace tree scheme but it is slightly faster by cause fewer hardware required.
- The Wallace scheme is hardware design which is used in digital systems.It normally multiplies two binary integers.The conventional Wallace tree multiplier infrastructure comprises of an AND array for determining the partial products, a carry save adder for adding them and finally a conventional fast adder is there be used in the final stage of addition.

Now a days there is a scope of advance technology in which the design of more efficient multiplier is dominant part of digital system [10]. The paper aims at offering higher speed and low power consumption even while occupying reduced silicon area. Subsequently, tradeoffs between area and delay parameters for each multiplier design are also analyzed for the different scheme. This makes them well-suited for several complex and portable VLSI circuits. In this paper the comparative study of Booth multiplier, Dadda multiplier,Wallace Tree multiplier is there by analyzing area, power and delay characteristics with particular importance on low power. The remaining part of the paper is described as follows: The literature review on Booth multiplier, Dadda

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multiplier,Wallace Tree multipliers is discussed in section III. The comparative analysis of these three multipliers is discussed in section IV. Finally results and conclusion are analyzed in section V and section VI respectively.

III. Literature Review

This literature survey presents a simple approach to reduce the power, area and delay of Booth Multiplier, Dadda tree Multiplier and Wallace tree Multiplier.

A. *Booth Multiplier*

Booth Multiplier uses booth encoding technique which provided to the generator program as user parameters. Booth encoding technique reduce the number of the additions for increase the speed of multiplication. It is a dominant algorithm for signed-number multiplication. Booth encoding is a technique, for reducing the number of partial products, required to produce the multiplication.For the standard add-shift operation, each multiplier bit generates one multiple of the multiplicand to be added to the partial product[8]. Basically the number of additions is determined delay of multiplier.

The advantage of this method is making the number of partial product into half of multiplier.The disadvantage is its complexity of the circuit to produce partial product. Booth algorithm is a method that will reduce the number of multiplicand multiples.

Example of Booth Encoding multiplier is shown in figure 3,in which add-shift operation,multiplier bit generation of multiplicand and multiplier and partial product addition operation can be performed conveniently.

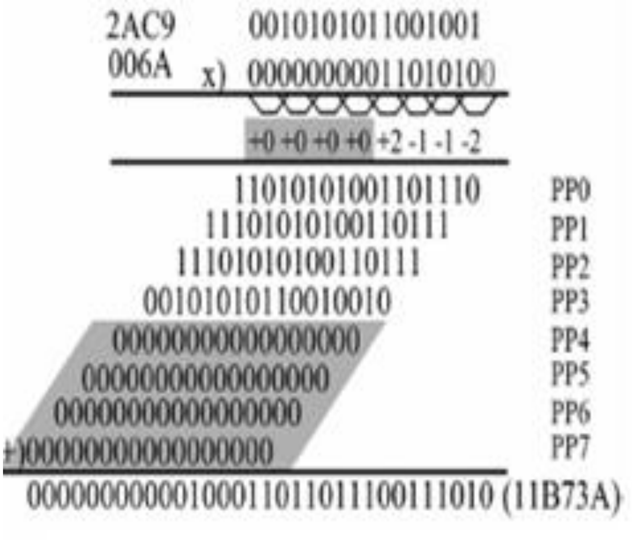

Figure 2. Example of Booth Encoding multiplier

This algorithm specify examination of the multiplier bits, and shifting of the partial product. Prior to the shifting, the multiplicand may be added to partial product, subtracted from the partial product, or left unchanged [12].

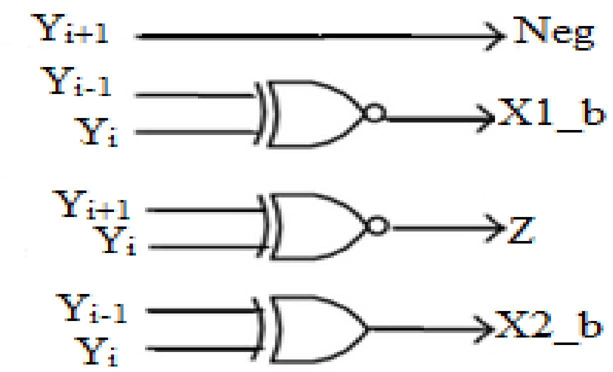

Figure 3. Booth encoder

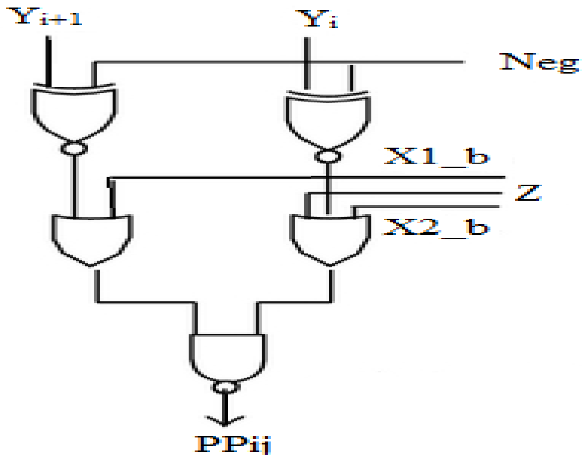

Figure 4. Booth decoder

The most common form of booth's algorithm looks at three bit of multiplier at a time to perform two stages of multiplication.

B. *Dadda Tree Multiplier*

Dadda multiplier perform the minimum reduction of partial products at each level.Column compression multiplier continued to be considered due to their high speed performance[10].

Dadda multipliers have the same 3 steps:

1. Multiply each bit of one of the arguments, by each bit of the other, yielding N2 results.

2. Reduce the number of partial products to two layers of full and half adders.

3. Group the wires in two numbers, and add them with a conventional adder.

Dadda multipliers perform few reductions only when compared to Wallace multiplier. Because of this, Dadda multipliers have less expensive reduction phase, but the numbers may be a few bits longer, thus requiring slightly bigger adders Dadda cultivated Wallace's method by defining a counter placement approach that required fewer counters in the partial product reduction stage at the cost of a larger carry-propagate adder. The Dadda reduction multiplier for 8 bit shown in figure 5.

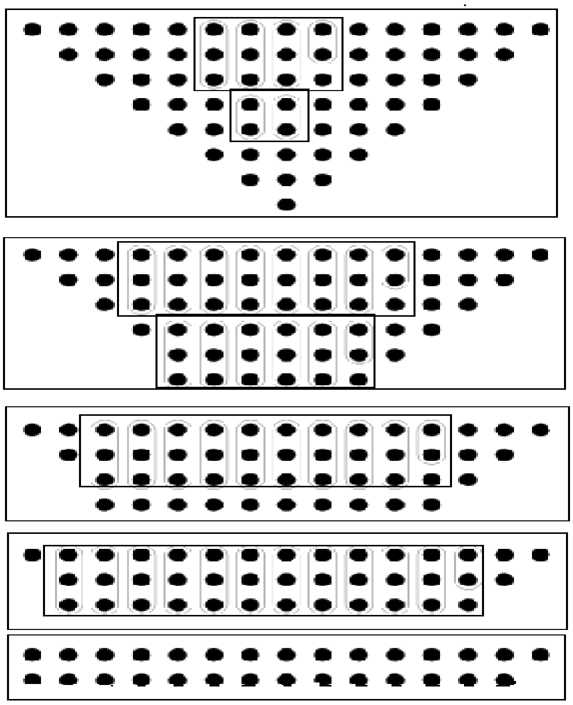

Figure 5. Dadda reduction in 8*8 multiplier

Dadda has introduced a number of ways to compress the partial product bits using such a counter which later became known as Dadda’s Counter [12]. Then it is observed that Dadda multiplier consumes less area as compared of Wallace tree multiplier.For both methods, the total delay is proportional to the logarithm of the operand word-length. There are number of stages in Dadda multiplier shown in table II.

TABLE I. NUMBER OF STAGES IN DADDA MULTIPLIER

Bit width of multiplier (N)	Stages (S)
2	0
3	1
4	2
5 to 6	3
7 to 9	4
10 to 13	5
14 to 19	6
20 to 28	7
29 to 42	8
43 to 63	9
64 to 94	10

In this paper we identify techniques for column compression multipliers by analyzing area, power and delay characteristics with particular emphasis on low power [19]. A direct approach is to use an M+1 bits carry propagate adder (CPA) to add the first two partial products, then another CPA to add the third partial product to the running sum, and so forth shown in figure 6.

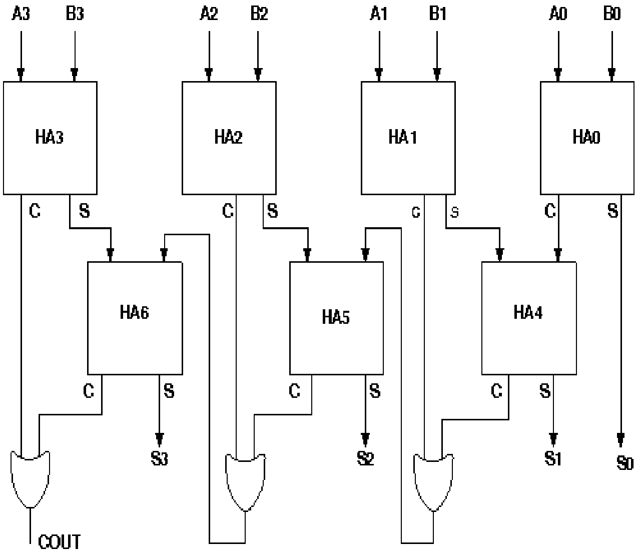

Figure 6. Carry propagate adder

Dadda tree multiplier provide a less area as compared to Wallace tree multiplier. For 8 bit size, the Dadda multiplier uses 7 half adders and 35 full adders. It is generally assumed that Wallace tree multiplier and Dadda tree multiplier shows same timing ,because each uses the same number of pseudo adder level to perform partial product reduction.The partial product matrix is formed in the first stage by N^2 AND stages. The Dadda multiplier design yields a slightly faster multiplier due to CPA.

The Dadda tree multiplier which made by half adders and full adders shown in Figure 7

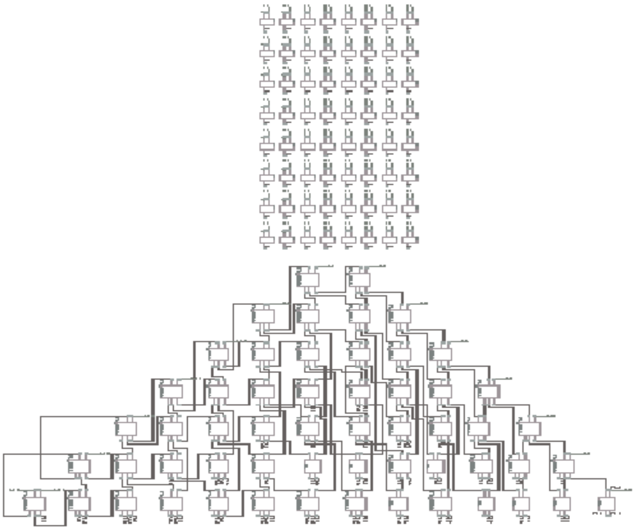

Figure 7. Dadda tree multiplier

C. *Wallace Tree Multiplier*

Wallace Tree multiplier design has been an essential multiplier in low- power VLSI design. In high-speed designs, the Wallace tree construction method is usually used to add the partial products in a tree-like fashion in order to produce two rows of partial products that can be added in the last stage.

In digital VLSI design, power-delay product is commonly used to measure the qualities of designs. This can be shown as power × delay = energy. The literature review will high lighting on the systematic study carried. In CPA (carry propagate adders); the long wires are required to propagate carries from low order bit to higher order bit. So this type of adder is comparatively slow in terms of speed. Therefore, CPA has the lowest speed amongst all the adders because of large carry propagation delay.A single carry propagate addition is only required in the last step to reduce the two numbers to a single, final product.The main object to get partial product accumulated by reducing the number of bits of information in each column using full adders or half adders.

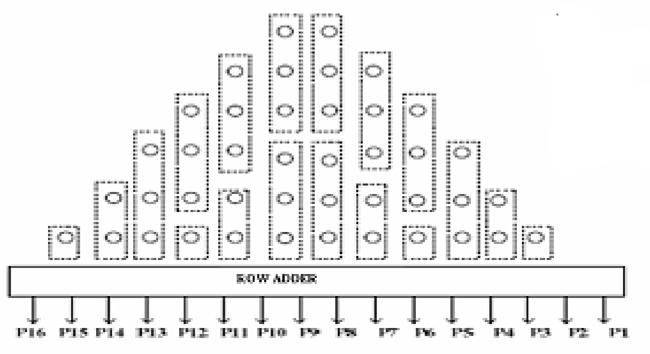

Figure 8. Block diagram-operation of 8-bit high speed wallace tree multiplier

The arrangement of this method is looks like a tree structure so this method is known as Wallace Tree multipliers. The block diagram of 8 bit high speed wallace tree multiplier is shown in figure 4 which specify the addition process for one column of partial products.

For different number of bits there are various number of reduction stages, shown in table I.

TABLE II. STAGES FOR WALLACE TREE MULTIPLIER

Number of bit in multiplier	Number of reduction stages
3	1
4	2
4<n<=6	3
6<n>=9	4
9<n<=13	5
13<n<=19	6
19<n<=28	7
28<n<=42	8
42<n<=63	9

There are basically three stages are used to multiply two numbers by using this method which described as: (1)Development of bit products (2) Reduction of the bit product (3) Addition of remaining two rows using a faster Carry Propagation Adder (CPA).

IV. Comparative Analysis Of Fast Multipliers

In the Area-Optimized mode, Radix-4 Booth Encoding multiplier has the lowest gate level logic value in all three of the Area-Optimized, Speed-Optimized and Auto-Optimized mode. However, there is a difference in the findings on which type of multiplier gives the largest gate level logic performance. Wallace multiplier exhibited the largest area in the Area-Optimized and Auto-Optimized modes while Dadda multiplier displays the lowest area performance in the Speed-Optimized mode. The modified tree has a slightly smaller critical path, a slightly larger wiring overhead but gives high speed. The most important works in this paper are study of multiplier design for high speed digital signal processing applications, identify the specifications for the multiplier design.The multipliers have been synthesized setting a constraint on speed to a maximum an operating frequency of 152.5MHz at 1.2V.

The following table shows the comparisons of different multipliers based on Area, Power and timing analysis.

TABLE III. COMPARISON OF MULTIPLIERS

BIT LENGTH (8 BIT)	**AREA (μM^{2})**	**POWER (μW)**	**DELAY (nS)**
BOOTH MULTIPLIER	5266.78	378.33	3.98
DADDA TREE MULTIPLIER	1395.79	645.60	1.72
WALLACE TREE MULTIPLIER	1315.15	678.43	1.73

V. Results

This paper review work compares three different multipliers- Booth multiplier,Dada tree and Wallace tree for 8-bit. The analysis is done on the basis of certain performance parameters i.e. Area, Power and delay.By comparison it observed that the modified Wallace tree is the best in terms of area and power. Using Xilinx tool comparison result also shows that a significant reduction of power is achieved.Table III shows the comparison between these three multiplier.Booth multiplier consumes less power comparative than Wallace tree and Dadda multiplier while it has maximum number of flip-flops. Figure 11 shows that Wallace tree multiplier has less area and less delay as compared to Dadda and Booth Multiplier

[1].

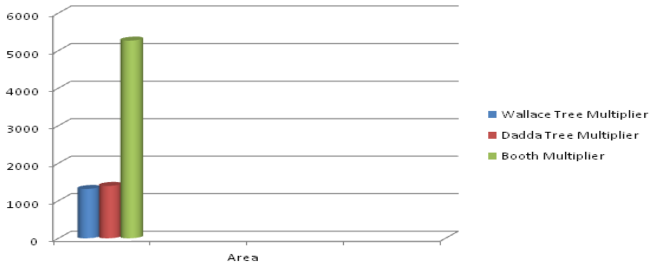

Figure 10 Comparison of multipliers for Area (μm^2)

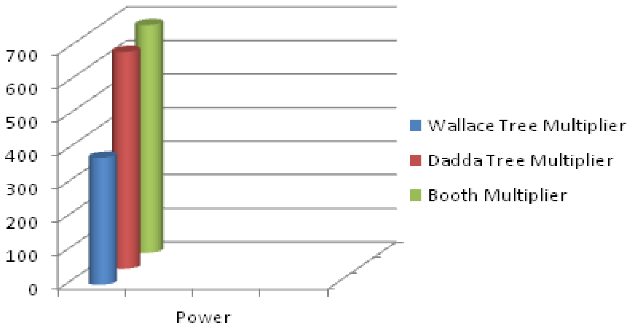

Figure 11 Comparison of multipliers for Power(μW)

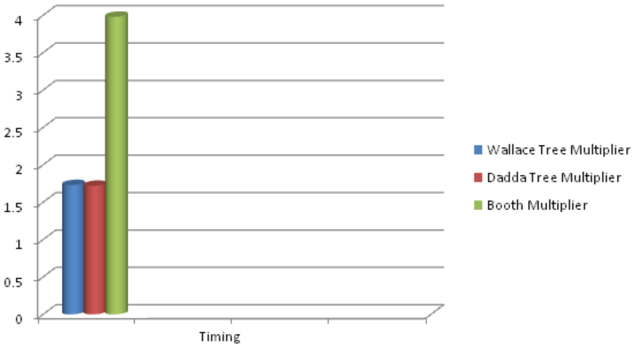

Figure 11 Comparison of multipliers for Delay (ns)

VI. Conclusion and Future Scope

Area, Power, and delay are the necessary factors in VLSI design that decide the performance. Area, Power, and delay comparison of multipliers is described, in this paper. This work proposes a simple and efficient approach to reduce the power, delay and area of Wallace tree multiplier architecture using different multipliers. These three multipliers are implemented using Xilinx tool and the area, power and timing are optimized of any digital circuit in low power digital circuits.This work is reviewed on 8-bit unsigned data. Therefore it can be extended for higher number of bits. for the rapid advances in multimedia and communication systems, FIR filters, digital signal processor, microprocessors etc. Many current DSP applications are targeted at portable, battery-operated systems, so that power dissipation becomes one of the primary design constraints.

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