Simulation and THD Analysis of Cascaded H-bridge Multilevel Inverter Topology

Sharad Patel, Pushpak Patel, Vishal Darji

***Abstract*— Cascaded H-bridge multilevel inverter is one of the popular converter topologies used in high power medium voltage application. Multilevel Inverter technology has emerged recently as a very important alternative in the area of high power, high voltage energy control. So multilevel inverter have been widely used for high power-high voltage drive applications. Due to higher number of sources, lower EMI, lower percentage (%) THD in output voltage and less stress on insulation. It is composed of a multiple units of single phase H-bridge power cells. The H-bridge cell are normally connected in cascade on their ac side to achieve medium voltage operation and low harmonic distortion. The Cascaded H- bridge multilevel inverter requires a number of isolated dc supplies, each of which feeds an H-bridge stiff DC supply. The dc supplies are normally obtained from bridge rectifiers. Various inverter topologies are introduced two carrier-based PWM schemes, phase-shifted and level Shifted modulations, are analyzed and their performance is compared. The simulation of cascaded H-bridge multilevel inverter by using the control scheme of multilevel inverter in PSIM. In the result of simulation of 5-level CHB multilevel inverter, the comparison of THD of inverter by various PWM scheme like as APOD and IPD and the THD of IPD PWM scheme are less compare to the APOD.**

***Index Terms*—- %THD,CHB multilevel inverter, carrier-based PWM schemes, IPD, APOD**

I. INTRODUCTION

Basically Inverter is a device that converts DC power to AC power at desired output voltage and frequency. Demerits of inverter are less efficiency, high cost, and high switching losses. To overcome these demerits, we are going to multilevel inverter. The term Multilevel began with the three-level converter. In recent years multi level inverters are used high power and high voltage applications .Multilevel inverter output voltage produce a staircase output waveform, this waveform look like a sinusoidal waveform. The multilevel inverter output voltage having less number of harmonics compare to the conventional bipolar inverter output voltage. If the multilevel inverter output increase to N level, the harmonics reduced to the output voltage value to zero. The multilevel inverters are mainly classified as Diode clamped, Flying capacitor inverter and cascaded multi level inverter. The cascaded multilevel control method is very easy when compare to other multilevel inverter because it doesn't require any clamping diode and flying capacitor. There are two PWM methods mainly used in multilevel inverter control strategy. One is fundamental switching frequency and another one is high switching frequency. For high switching frequency classified as space vector PWM, Selective Harmonics Elimination PWM and SPWM. Among these PWM methods SPWM is the most used for the multilevel inverter, because it has very simple and easy to implemented. In this paper present SPWM method with the different carrier based disposition IPD, POD and APOD PWM has been analyzed. It is generally accepted that the IPD strategy gives rise to the lowest harmonic distortion for the line-to-line voltage. Any semiconductor switches have already been proposed. In this proposed concept uses the MOSFETs semiconductor switches. MOSFETs are preferred in High frequency applications (1MHZ), Wide load variations, Long duty cycles, and Low-voltage applications (100V). Mainly selected the MOSFET switches are used because of its fast switching capability.

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II. 3-PHASE 5-LEVEL CHB MULTI LEVEL INVERTER

The cascade inverter in the figure, can produce a phase voltage with five voltage levels. The resultant inverter phase voltage is UAN = UH1 + UH2, which is the voltage at the inverter terminal A with respect to the inverter neutral N. The output voltage can be 0, ±E, ±2E. The voltage levels which correspond to various switching states are summarized in table. It can be observed from the table that some voltage levels can be obtained by more than one switching state. These redundancies are common in multilevel inverters. It provides a great flexibility for switching pattern design, especially for space vector modulation schemes. In a general way If H is the number of single-phase H-bridges per phase, the number of levels of the inverter is:

$$\mathbf{m= (2H+1)}$$

where, H is the number of H-bridge cells per phase leg. The voltage level m is always an odd number for the CHB inverter. The CHB inverter introduced above can be extended to any number of voltage levels. The per-phase diagram of seven- and nine-level inverters are depicted in Fig.3.9, where the seven-level inverter has three H-bridge cells in cascade while the nine-level has four cells in series. The total number of active switches (IGBTs,MOSFETs) used in the CHB inverters can be calculated by,

$$\mathbf{Nsw = 6(m – 1)}$$

Where, **Nsw** is total number of switches and **m** is a voltage level.

Advantages:

- The multilevel inverter is composed of multiple units of identical H-bridge power cells, which leads to a reduction in manufacturing cost
- Lower voltage THD and dv/dt. The inverter output voltage waveform is formed by several voltage levels with small voltage steps. Compared with a two-level inverter, the CHB multilevel inverter can produce an output voltage with much lower THD and dv/dt.

Disadvantages:

- High component count. The CHB inverter uses a large number of MOSFETS modules. A five-level CHB inverter requires 24 MOSFETS with the same number of gate drivers.
- Large number of isolated dc supplies. The dc supplies for the CHB inverter are usually obtained from a stiff DC supply employing an expensive phase shifting transformer.

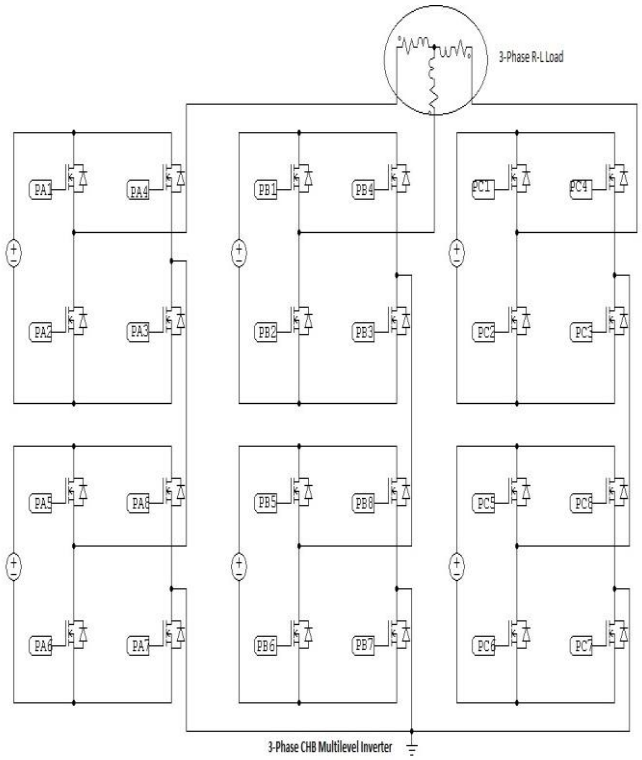


Figure 1: 3-phase CHB multilevel Inverter

In this diagram, the 24 no. of MOSFETS are used and after that get the output 5 level voltage. The output is given to the 3-Phase load like as R-L load taken normally. The pulses are generating by comparing the triangular wave and sinusoidal wave. For 5 level output ,the triangular wave are taken N-1. Means 4 triangular waveform required. Which are compare to sinusoidal waveform and pulse are given to the each MOSFET with necessary deadband.

Table 1

Output voltage VAN	S11	S31	S12	S32	VH1	VH2
2E	1	0	1	0	E	E
E	1	0	1	1	E	0
	1	0	0	0	E	0
	1	1	1	0	0	E
	0	0	1	0	0	E
0	0	0	0	0	0	0
	0	0	1	1	0	0
	1	1	0	0	0	0
	1	1	1	1	0	0
	1	0	0	1	E	-E
	0	1	1	0	-E	E
-E	0	1	1	1	-E	0
	0	1	0	0	-E	0
	1	1	0	1	0	-E
	0	0	0	1	0	-E
-2E	0	1	0	1	-E	-E

III. LEVEL SHIFTED MODULATION SCHEME:

1) In Phase Disposition (IPD)

For the scheme based on phase disposition it has been found that the THD obtained are 6.51% and 3.19% for the phase and line to line voltages respectively.

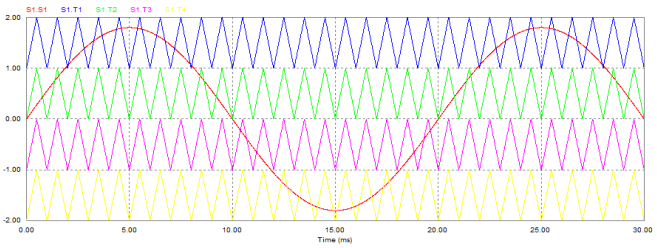


Figure 2: IPD PWM Scheme

2) Phase opposite Disposition (POD)

For the scheme based on phase opposite disposition it has been found that the THD obtained are 6.56% and 5.61% for the phase and line to line voltages respectively.

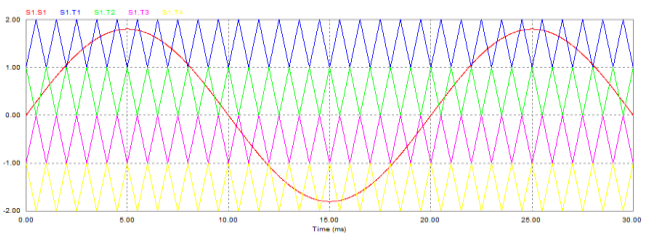


Figure 3: POD PWM Scheme

3) Alternative Phase opposite Disposition (APOD):

The THD obtained are 5.68% and 5.61% for the phase and line to line voltages respectively.

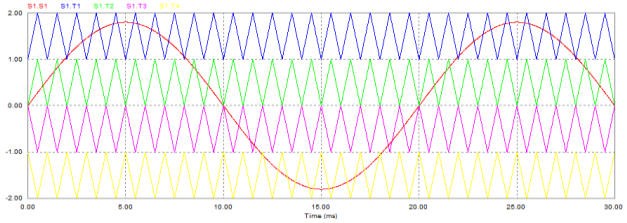


Figure 4: APOD PWM Scheme

The different modulation schemes explain above, in phase disposition (IPD) presents the lowest THD of the line to line voltage.

IV. SIMULATION RESULTS:

In this section the simulation results for five-level inverter using cascaded H-Bridge topology are demonstrated by PSIM6.0 software module. For single-phase five-level inverter and for three-phase five-level inverter the dc source voltage is 50 V, and frequency of carrier signal is 1 kHz. In this topology, in the carrier based implementation the in phase disposition PWM (IPD) scheme is used, where the carrier waveforms are in phase with the reference waveform. In inverter the number of carriers used are N-1 so four carrier waveforms are needed to design a five-level inverter.

V. SINGLE PHASE 5-LEVEL CHB MULTILEVEL INVERTER

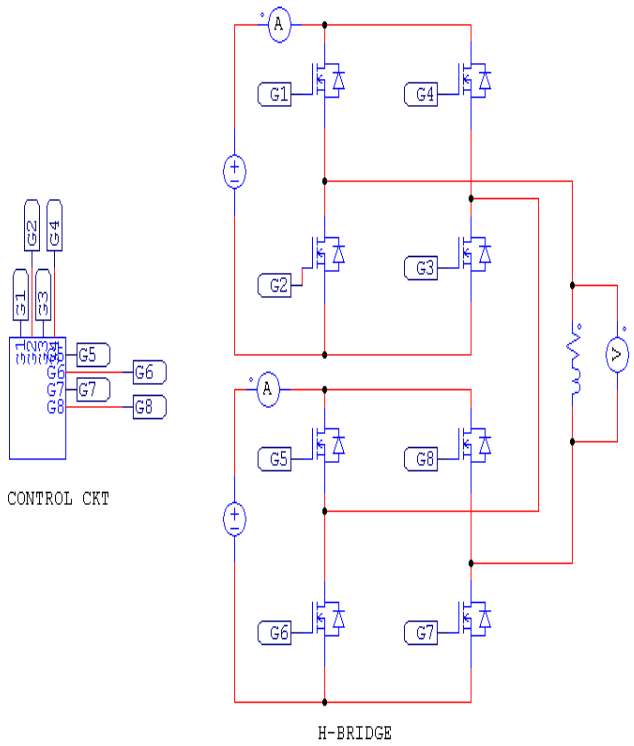


Figure 5: Simulation of 1-Phase CHB Inverter

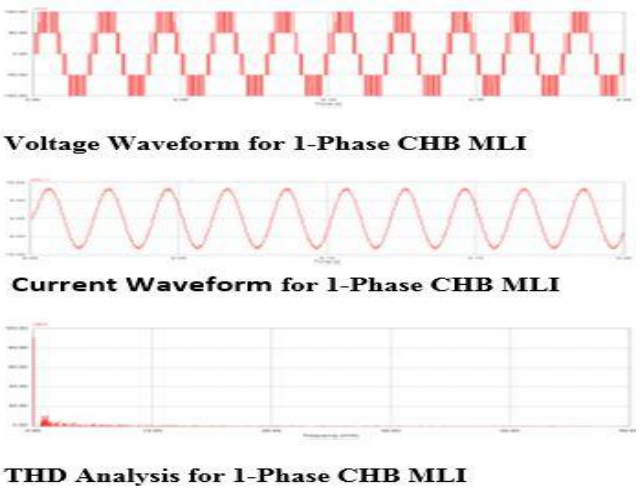


Figure 6: Voltage and current Waveform And THD Analysis

The fig. 9 shows the result from simulation of five-level inverter on R-L load. Here R = 10 Ω and L = 15 mH. Simulation is done keeping modulation index m = 0.8. The load current is very close to the sinusoidal waveform. Normalized harmonic spectrum of output voltage is shown in fig. It is evident that it does not contain any lower order harmonics.

VI. THREE PHASE 5-LEVEL CHB MULTILEVEL INVERTER

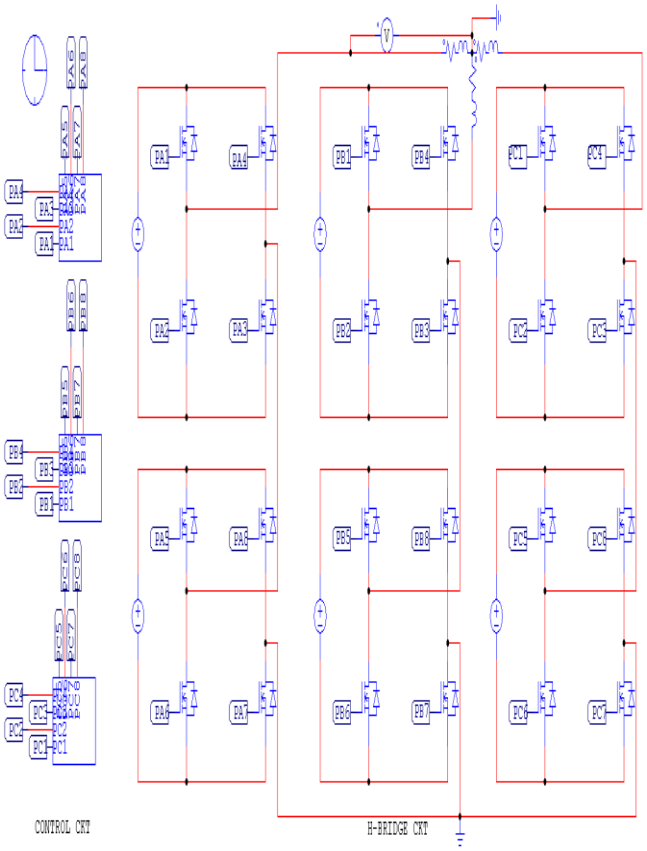
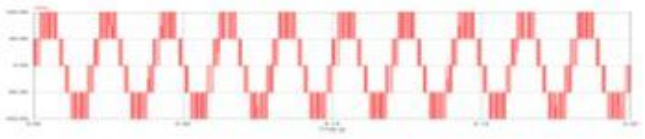
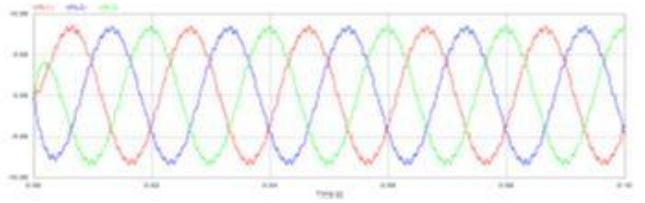


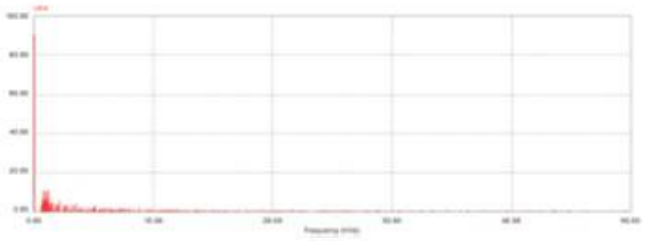
Figure 7: Simulation of 1-Phase CHB Inverter



Voltage Waveform for 3-Phase CHB MLI



Current Waveform for 3-Phase CHB MLI



THD for 3-Phase CHB MLI

Figure 8: Voltage and current Waveform And THD Analysis

VII. CONCLUSION

Simulation results illustrate the performance and effectiveness of single phase and three phase 5 level cascaded H-bridge multilevel inverter of the proposed circuit for R-L load, getting the result of 5 level voltage and current wave form by In Phase Disposition (IPD) PWM scheme. The load current is very close to the sinusoidal waveform. After the THD comparison of IPD and APOD, there is a less THD by using IPD pwm schemes. So, concluded that IPD is much better than APOD for the practical approach. And the second simulation for 3-phase 5 level cascaded H-bridge multilevel inverter, also we get the 5 level output voltage and current. The load current is very close to the sinusoidal waveform.

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