

# Simulation and Analysis of Sense Amplifier in Submicron Technology

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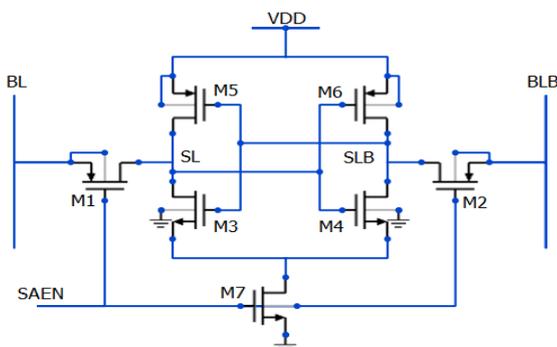
**Abstract**— When density of memory is increased, the bit line capacitance is also increases and due to that, it limits the speed of voltage sense amplifier. To overcome this problem current sense amplifier is used, which is not dependent on bit line capacitance. In this paper voltage mode sense amplifier, current latch sense amplifier and current sense amplifier is analyzed and simulated in a 45nm process technology using Ngspice circuit simulator. This paper shows that delay time is reduced in current sense amplifier compare to voltage mode sense amplifier and current latch sense amplifier but power consumption is increased.

**Index Terms**— SRAM, Sense amplifier, Cross coupled Voltage mode sense amplifier, Current latched sense amplifier , Current sense amplifier.

## I. INTRODUCTION

SRAM is used at where high speed and high performance microprocessor is used. Simultaneously SRAM is also used at where low power is required. When number of SRAM cell is increased to store large number of data, it becomes necessary to use sense amplifier. Sense amplifiers detect the data being read by sensing a small differential voltage swing on the bit-lines rather than waiting for a full rail-to-rail swing. Depending on the performance and power requirements, it's very important for the sense amplifiers to operate fast and do so while burning a minimum amount of power. The large bit-line capacitance is a big performance bottleneck. The amount of time required to develop this differential voltage is linearly proportional to bit-line capacitance. Conventional Voltage Sense Amplifiers need a minimum amount of differential voltage to be developed on the bit-lines for reliable operation.

## II. VOLTAGE MODE SENSE AMPLIFIER



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Fig.1. “Cross-coupled voltage mode SA<sup>[2]</sup>”

Fig.1 shows the schematic of Cross-coupled voltage mode SA. M1 and M2 are the access transistors, whereas M3-M6 forms cross-coupled inverters. When SAEN is low, M1 and M2 are turned ON and voltage on BL and BLB will be transferred to SL and SLB respectively. Due to positive feedback, higher voltage level goes to VDD and other level goes towards zero. In the basic cross-coupled SA, the nodes SL and SLB are input and output terminals simultaneously at one time. Hence, the circuit is not be connected directly to the bit line since the circuit would attempt to discharge the bit line capacitance during the decision phase and would increase delay and power<sup>[5]</sup>.

The NMOS devices M3 and M4 in the cross coupled inverter pair as well as the enable device M7 need to be sized for speed since they are in the critical discharge path. Speed is improved if the M7 device is sized higher. But higher widths on M3 and M4 are very important due to process variations. The initial voltage difference at the output nodes created by bit-line voltage difference may not result in the flipping of the cross-coupled inverters in the right direction if there is sufficient trip point voltage.

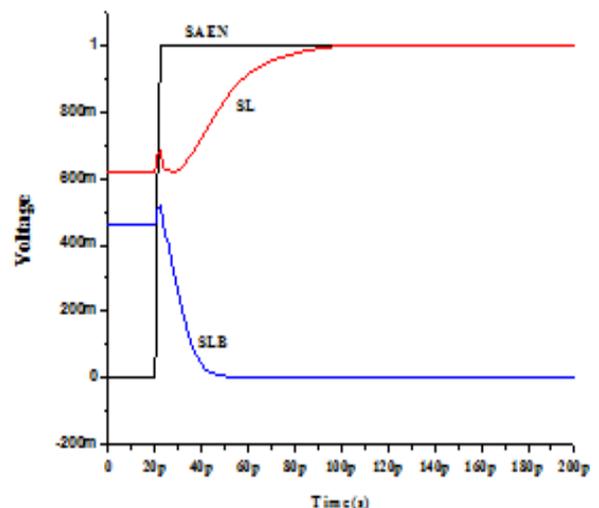


Fig.2. “Simulation result of Cross coupled VSA”

Up sizing widths of M3 and M4 is effective in reducing the failure probability because it reduces  $V_t$  variation and hence trip point mismatch<sup>[4]</sup>. Increasing the width of M7 does not lower failure probability because it is a common transistor for the two paths and its variation affects both paths equally.

III. CURRENT LATCH SENSE AMPLIFIER

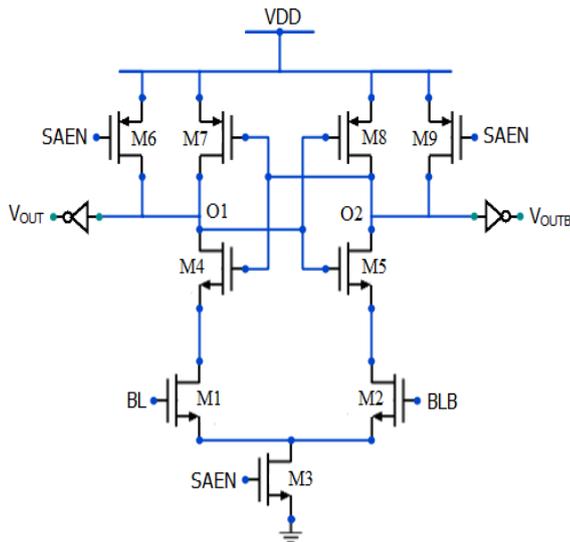


Fig.3 . “Current latch sense amplifier” [3].

The current flow of the differential input transistors M1 and M2 controls the serially connected latch circuit. This current latched SA is faster than conventional cross coupled SA. During reset phase when SAEN=0V, the output nodes of the SA (O1 and O2) are reset to VDD through the reset transistors M6 and M9. During evaluation phase when SAEN=VDD, M3 turns ON and the input transistors M1 and M2 starts to discharge O1 and O2 node voltages to GND. When any of these node voltages falls from VDD to  $V_{DD}-V_{thn}$ , NMOS transistors of the cross coupled inverters turn ON initiating positive feedback. Further when any of output node voltage drops to  $V_{DD}-V_{thp}$ , PMOS transistors of the inverters turns ON and further enhances the positive feedback and converts a small input voltage difference to large full scale output. Inverters are used further to speed up the sensing process. Fig. 3 shows simulation results of current latched sense amplifier trying to read data of memory cell containing logic ‘1’. When word line WL is high to access the memory cell, BLB starts to discharge from VDD and BL remains high. After SAEN is asserted, cross coupled inverters amplify small differential voltage between bit lines to full rail output as shown in Fig.3.3. Here, due to higher BL voltage M1 has higher current. So, O1 discharges faster than O2 and we get logic high after inverted by inverter.

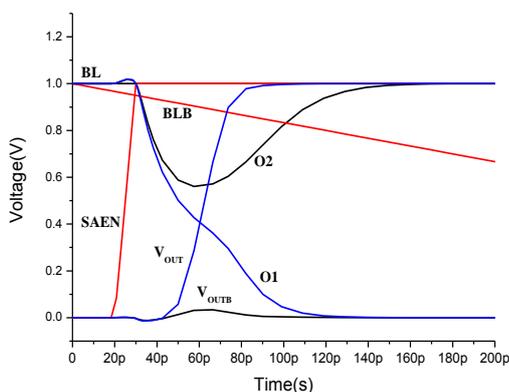


Fig.4. “Simulation result of CLSA”

IV. CURRENT SENSE AMPLIFIER

The current sense amplifier operates in two phases: pre charge and evaluate. During the pre charge phase, the bit-lines are pre charged through pre charge devices connected to the bit-lines. The Output nodes SA and SA# are also pre charged high through M11 and M12 PMOS devices. The operating current of the sense amplifier is determined by the sizes of devices M5-M8. At the end of the pre charge phase, pre charge and equalization devices M11-M13 are turned OFF. During the evaluation phase, Ysel is pulled low and current is immediately transported to the nodes A and B through the drains of M3 and M4. The difference in current flowing through A and B will be equal to the cell current. The sense amplifier is enabled two-inverter delay after the SAen is pulled high during which bias current flows through two legs of the sense amplifier, while M14 keeps the output equalized. After this two inverter delay, M14 is disabled and the differential current causes a differential voltage to be developed at SA and SA#. This differential voltage is then amplified to CMOS logic levels by the high-gain positive feedback cross-coupled inverters formed by M5-M8.

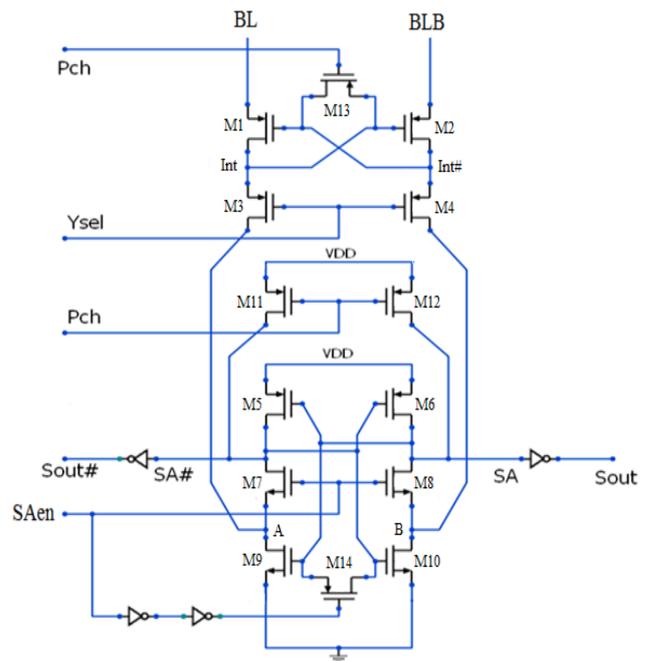


Fig.5. “Current sense amplifier” [1].

The sensing delay is relatively insensitive to bit-line capacitance as the operation is not dependent on the development of a differential voltage across the bit-lines. The CSA have low voltage swing on bit-lines. This is because the cross coupled PMOS pair M1 and M2 cuts off the discharge path to ground for both bit-lines. If BL is high and BL# is low. This causes nodes Int and A to go high causing M2 to be cut off. Therefore, the path from the low going BL# to ground is cut off, reducing the voltage swing on it. This scheme enhances the speed of the sense amplifier further due to the fact that there is a flow of bias current before the sense

amplifier is actually enabled. This results in small increase in the static power consumption [1].

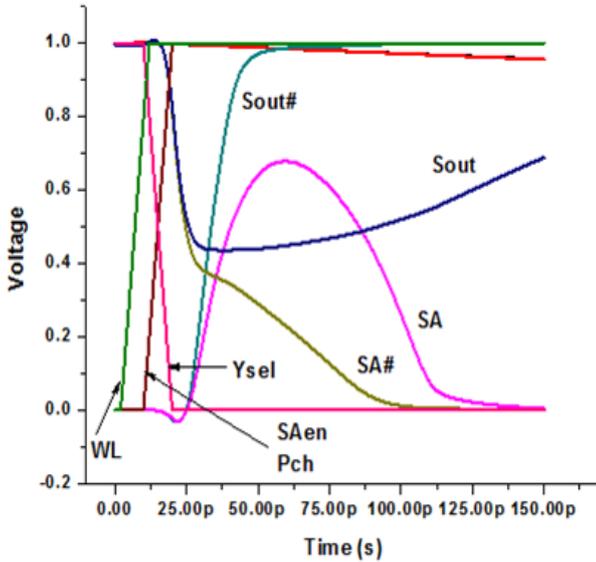


Fig.6. "Simulation result of CSA"

#### V. PERFORMANCE SUMMARY OF SA

All three types of sense amplifiers are simulated in 45nm technology using NGSPICE. Table 1, shows performance summary of these sense amplifiers.

Table1. "Comparison of different types of SA"

Parameter	Cross Coupled VSA	Current Latched SA	Current SA
Delay( ps)	58.62	33.06	18.5
Cell Current (μA)	38.41	73.36	241.76
Power Dissipation (μW)	38.41	73.36	241.76
Power delay product(fj)	2.25	2.42	4.47

#### VI. CONCLUSION

Cross Coupled VSA , Current latched SA and Current SA is analyzed and simulated and that analysis show that sensing delay time in Cross coupled VSA is 80.33 % higher than CLSA but power dissipation is 90.99% lower than CLSA. Sensing delay time in CLSA is 78.70% higher than CSA but power dissipation is more lower than CSA. Power delay product(PDP) is a figure of merit for digital technology. The design goal is to minimize PDP in order to get low power in high frequency. Cross coupled VSA consist lower PDP than CLSA and CSA.

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#### ABBREVIATION

- SRAM : Static random access memory  
SA : Sense amplifier  
VSA : Voltage sense amplifier  
CLSA : Current latch sense amplifier  
CSA : Current sense amplifier