Simulation and analysis of Bulk Driven Circuits for Low Power Applications

Trupti B. Desai, Pratik P. Shah

***Abstract*— In this paper, low voltage low power (LV LP) integrated circuits design based on bulk-driven MOSFET are presented. This paper is devoted to the Bulk-driven principle and this principle is used to design LV LP building blocks of Current Mirror (CM), Cascode Current Mirror (CCM).The proposed circuits are simulated using SPICE for 0.180µm CMOS technology and their results are compared with that of conventional Current Mirror , Cascode Current Mirror.**

***Index Terms*— Bulk-driven MOSFET, Current Mirror (CM), Cascode Current Mirror (CCM).**

I. INTRODUCTION

In the last few decades where the market for portable electronic systems such as a wireless Communication devices, hearing aids, consumer electronics, etc. is continuously expanding, there is a growing need for the development of low-voltage (LV) and low-power (LP) circuit techniques and system building blocks. Both low-voltage and low-power operation are of great importance for portable applications. Low-voltage operation is demanded because it is desirable to use as few batteries as possible for size and weight considerations. Low-power consumption is necessary to ensure a reasonable battery lifetime. An important factor concerning analog circuits is that; the threshold voltages of future standard CMOS technologies are not expected to decrease much below what is available nowadays. The MOS transistor is a four terminal device; it is mostly used as a three terminal device since the bulk terminal is tied either to the source terminal otherwise to the drain terminal, to VDD or to VSS. So, a large number of possible MOS circuits are overlooked; hence a good solution to overcome the threshold voltage is to use the Bulk-driven principle [4]. The principle of the Bulk-driven is that; the gate-source voltage is set to a value sufficient to create an inversion layer.

An input signal is applied to the bulk terminal of the MOSFET. In this way, the threshold voltage can be either reduced or removed from the signal path. The operation of the Bulk-driven MOS transistor is much like a JFET i.e. a depletion type device, it can work under negative, zero, or even slightly positive biasing condition. The main advantage of the bulk-driven MOSFET over a Conventional MOSFET is that the threshold voltage requirements are removed from signal path.

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II. SIMPLE CONVENTIONAL CURRENT MIRROR AND BULK-DRIVEN CURRENT MIRROR

Current mirrors are one of the most common buildings Blocks both in analog and mixed-signal VLSI circuits. Current mirrors are very useful elements for Performing current-mode analog signal processing [7]. Current mirror consist of two branches that parallel to each other and create two approximately equal current. This is why these circuits are called Current Mirror. The principle of the Current Mirror is that if the gate-source potentials of two identical CMOS transistors are equal, then the current flow through their Drain terminals should be the same. The current mirror is used to provide biasing currents and active loads to the circuits.

A. Simple Conventional Current Mirror

The conceptual schematic of the Conventional current mirror is shown in Figure 1.

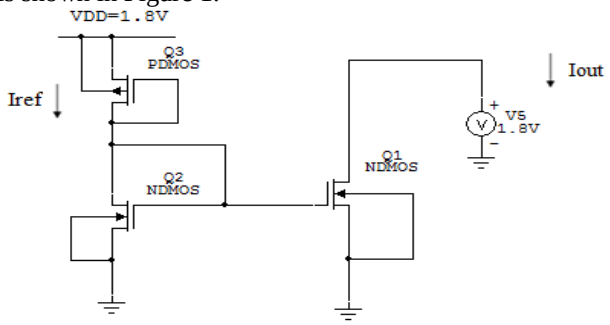

Fig.1."Simple Conventional Current Mirror" Circuit consisting of Q1, Q2, Q3 CMOS Transistor. Current I_{ref} is to be mirror by the Q1 through diode connected load Q2.For proper operation the aspect ratio of the both transistors are keeping same. As the drain and gate terminal of Q2 are tied together Vds2 is equal to the Vgs2. So Q2 operates in the saturation region and act as a diode connected load. Since gate to source voltage of Q1 is equal to that of Q2. Therefore for the same gate to source voltages their drain current also has to remain same. To overcome the threshold voltage from signal path Bulk-driven Current Mirror is used. Drain Current of the MOSFET is calculated by

$$i_D = \frac{KW}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \quad \text{for } V_{DS} \le V_{Dsat} \quad (2.1)$$

$$i_D = \frac{KW}{L}\left(V_{GS} - V_T\right)^2 (1+\lambda V_{DS}) \quad \text{for } V_{DS} \le V_{Dsat} \quad (2.2)$$

$$\text{Where } V_T = V_{T0} + \gamma\left(\sqrt{|2\emptyset_F| - V_{SB}} - \sqrt{|2\emptyset_F|}\right)$$

S0 final drain current equations of the bulk driven MOSFET is given by,

$$i_D = \frac{KW}{L}(V_{GS} - V_{T0} - \Upsilon\sqrt{|2\emptyset_F| - V_{SB}} + \Upsilon\sqrt{|2\emptyset_F|} - \frac{V_{DS}}{2})V_{DS}$$

for $V_{DS} \leq V_{Dsat}$ *(2.3)*

$$i_D = \frac{KW}{L}(V_{GS} - V_T - \Upsilon\sqrt{2\emptyset_F - V_{SB}} + \Upsilon\sqrt{2\emptyset_F})^2 (1+\lambda V_{DS})$$

for $V_{DS} \geq V_{Dsat}$ *(2.4)*

B. Bulk-Driven Current Mirror

The conceptual schematic of the Bulk-Driven Current mirror is shown in Figure 2.

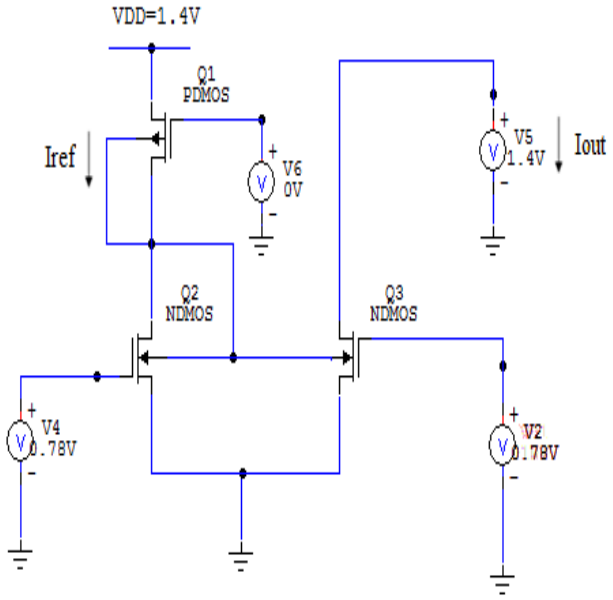

Fig.2. "Bulk-Driven Current Mirror"

Circuit consisting of Q1,Q2, Q3 CMOS Transistor. If the signal is applied to the bulk terminal instead of to the gate terminal and keeping VGS voltage of the MOSFET constant then device operate as bulk-driven MOS transistor. In bulk driven n-MOSFET, body to source voltage is kept lower than the switch on voltage of the diode, otherwise large forward current will flow from the device. In Bulk-driven current mirror, sufficient voltage is provided to the gate terminal to create the inversion layer and input signal is applied to the bulk terminal of the MOSFET.

III. CASCODE CURRENT MIRROR

Current mirror suffers from the channel length modulation effect so; load current does not follow the bias current exactly. For proper mirror current, gate driven Cascode current mirror is to be designed. Cascode current mirrors are used, to achieve high output resistance.

A. Gate-Driven Cascode Current Mirror

The conceptual schematic of the Gate-Driven Current mirror is shown in Fig. 3. It consists of Q1, Q2, Q3, Q4, Q5 CMOS transistor. I_{ref} current flows through the Q2 Transistor. I_{out} current try to follow the Iref current.

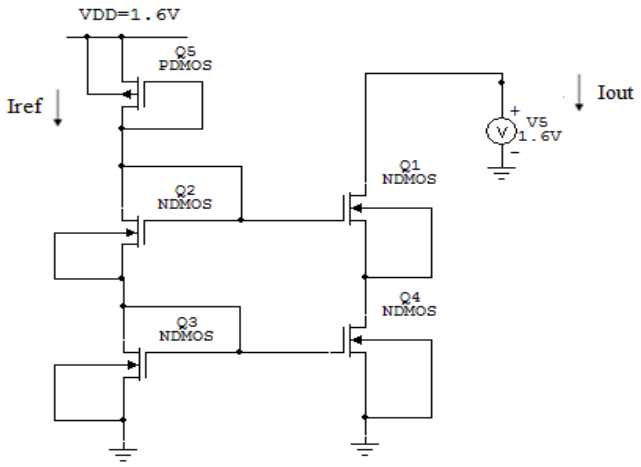

Fig.3. "Gate-Driven Cascode Current Mirror"

B. Bulk-Driven Cascode Current Mirror

The conceptual schematic of the Bulk-Driven Current mirror is shown in Figure 4.

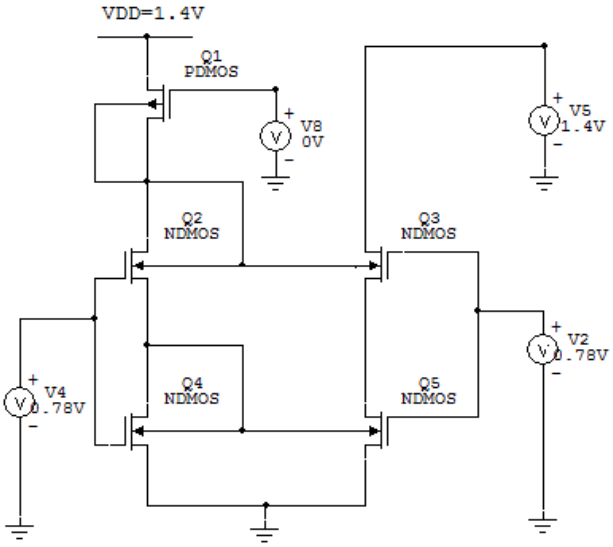

Fig.4. "Bulk-Driven Cascode Current Mirror"

If we apply signal to the bulk instead of to the gate, and keeping VGS constant then device operate as bulk-driven MOS transistor. Vbs2 = Vds2, and Vbs4 = Vds4. Q2 and Q4 operates in linear region which forces the Q3 and Q5 to operate in linear region, therefore I_{out} is forces to match Iref. CMOS transistor. I_{ref} current flows through the Q2 Transistor. I_{out} current try to follow the Iref current.

IV. SIMULATION RESULTS AND ANALYSIS

The above implemented proposed Conventional current mirror was simulated along with its gate driven equivalent in 180 nm CMOS process using NGSPICE Tool. Output voltage-Current Characteristic of Gate-driven Current Mirror is shown in Figure 5.

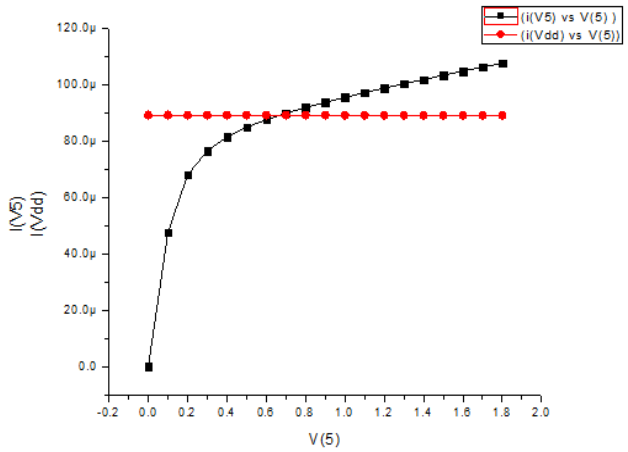

Fig.5. "Output voltage-Current Characteristic of Gate-driven Current Mirror"

For test setup Iref is set to 89uA, V_{dd} equals to 1.8V and V_{out} is vary from 0 to V_{dd} and corresponding I_{out} is measured and plotted for (W/L)Q2 = (W/L)Q1 equals to (0.180u / 2u). From simulation result shown in Fig.5. It can be observed that output current I_{out} is not exactly mirrored from the reference current I_{ref} is equals to 108uA due to channel length modulation CLM effect.

Output voltage-Current Characteristic of Bulk-driven Current Mirror is shown in Fig.6.

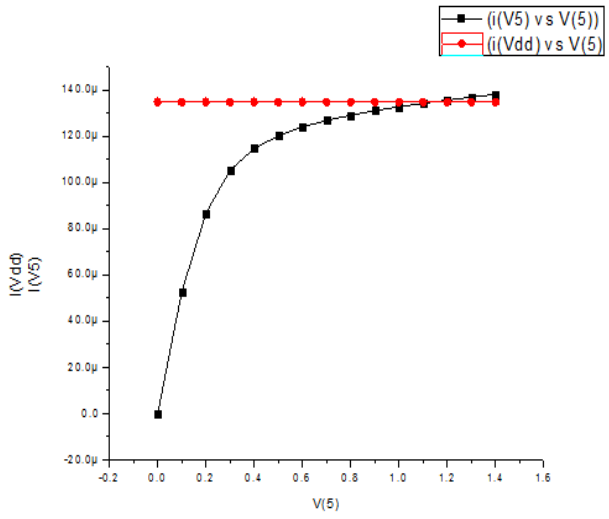

Fig.6. "Output voltage-Current Characteristic of Bulk-driven Current Mirror"

From simulation result shown in Fig.6, it can be observed that output current Iout is not exactly mirrored from the reference current Iref is equals to 138uA due to channel length modulation CLM effect but it give high current driving Capability compare to conventional current mirror.

Output voltage-Current Characteristic of Gate-driven Cascode Current Mirror is shown in Fig. 7.

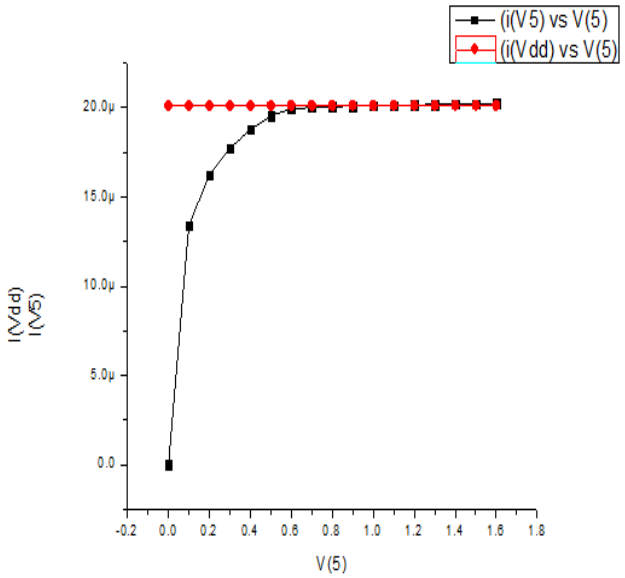

Fig.7. "Output voltage-Current Characteristic of Gate-driven Cascode Current Mirror"

From simulation result shown in Fig.7, it can be observed that output current Iout is 20uA exactly mirrored from the reference current Iref is equals to 20uA.

Output voltage-Current Characteristic of Bulk-driven Cascode Current Mirror is shown in Figure 8.

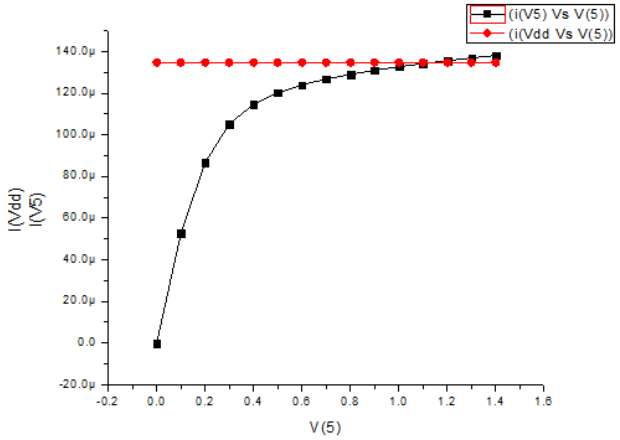

Fig.8. "Output voltage-Current Characteristic of Bulk-driven Cascode Current Mirror"

From simulation result shown in Fig.8, it can be observed that For bulk driven Cascode current mirror we can obtain the output current from 0.2V therefore we can say that bulk driven current mirror operate on lower supply voltage. Also the magnitude of output current of bulk driven current mirror is higher than gate driven current mirror. Table1. Shows the Comparison of voltage and current of various circuits

Table1. "Comparison of voltage and current of various circuits".

	GDCM	BDCM	GDCCM	BDCCM
Voltage(V)	1.8	1.4	1.6	1.4
Current(µA)	108	138	20	138

V. CONCLUSION

The Simulation result shows that the bulk-driven technique removes the threshold voltage limitation of MOSFETs from the signal path. Bulk-driven MOS transistors can operate at lower power supply voltage V_{dd} up to 1.4V. With such a low power supply voltage, designing analog circuit using conventional gate-driven MOS transistors is difficult. Different analog block has designed using the bulk driven techniques. Bulk Driven MOSFETs has high Current driving Capability compared to the Gate driven MOSFETs.

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ACRONYMS

CMOS Complementary Metal Oxide Semiconductor
GDCM Gate-driven current mirror
BDCM Bulk-driven current mirror
GDCCM Gate-driven Cascode current mirror
BDCCM Bulk-driven Cascode current mirror
CLM Channel length modulation
MOSFET Metal Oxide Semiconductor Field Effect Transistor
NMOS n-channel Metal Oxide Semiconductor Field Effect Transistor
PMOS p-channel Metal Oxide Semiconductor Field Effect Transistor